

A circular logo for the R4 Workshop 2024. The logo has a green border with the text "OCTOBER 3" at the top and "WORKSHOP 2024" at the bottom. Inside the border is a blue and purple gear pattern. In the center, the letters "R4" are written in a large, stylized font where the "R" is purple and the "4" is green.

Internals of the Intel Tofino Compiler

Glen Gibb, Intel

Introduction

This presentation provides an overview of the Intel Tofino compiler's internals.

I'll be primarily focusing on four major topics:

- Custom IR nodes
- PHVInfo – a data collection/query module
- Resource allocation (PHV and table)
- Backtracking

Company Overview

Intel produces the P4-programmable Tofino switch ASICs and the Intel IPU E2100.

Intel is best-known for their microprocessors, with their Xeon, Core, and Atom product lines powering many of today's computers.

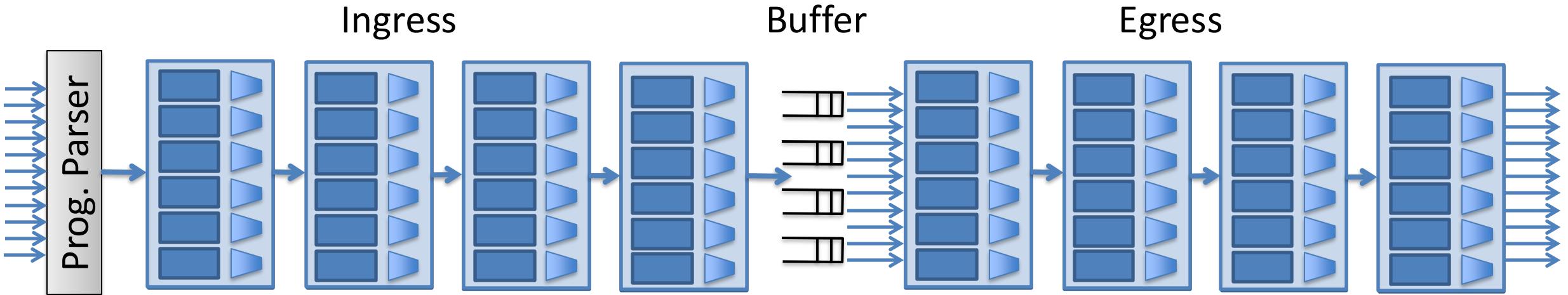
**Intel is open sourcing the
Tofino compiler**

(+ most of the software stack)

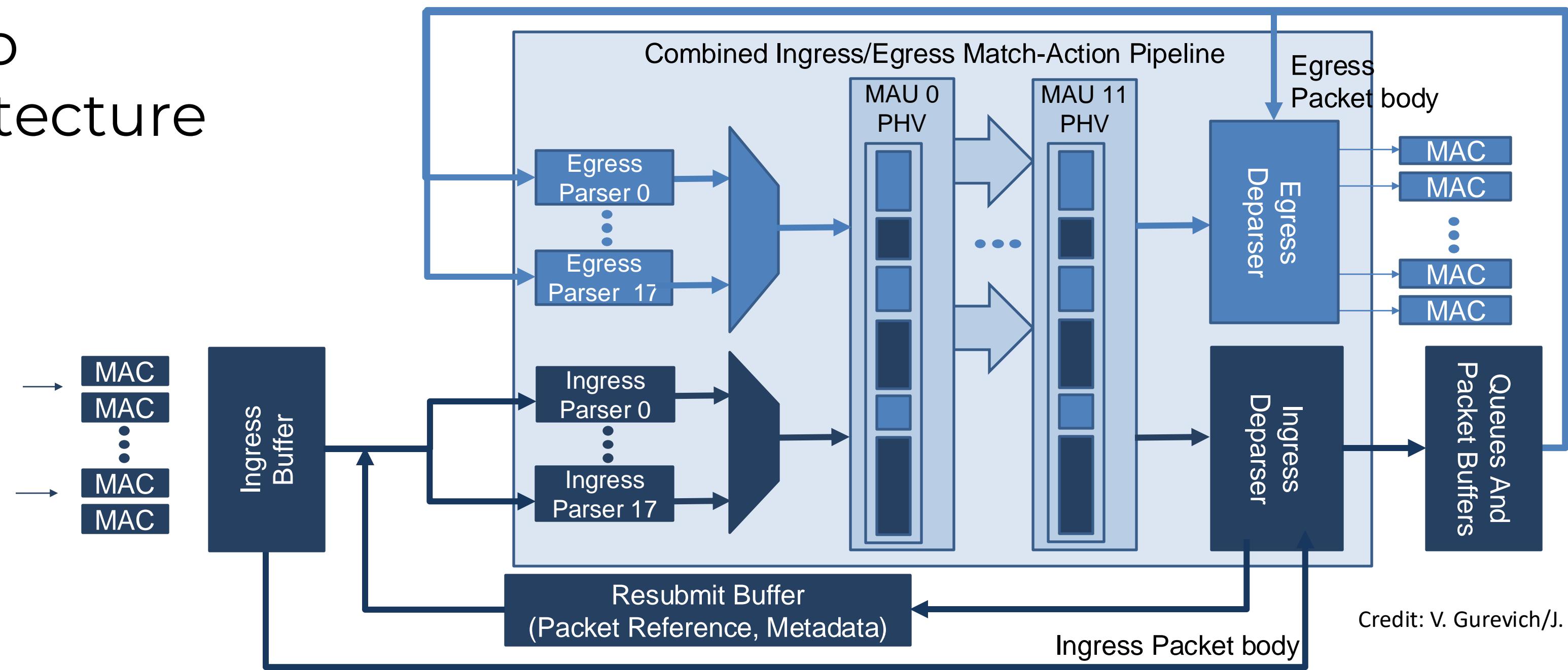
Outline

- Tofino architecture
- Midend/backend tour
- Tofino IR nodes
- PhvInfo / PHV::Field objects
- Resource allocation
- Backtracking

PISA: Protocol-Independent Switch Architecture



Tofino Architecture



Tofino architecture

- Match-Action Unit (MAU)
 - Implement multiple logical tables
 - Shared between ingress/egress
 - Allocatable resources
 - SRAMs
 - TCAMs
 - ALUs
 - Xbars
 - MAUs per pipe:
 - Tofino 1: 12
 - Tofino 2: 20
- Packet header vector (PHV)
 - Wiliide (4kb+)
 - 8b / 16b / 32b containers
 - Shared between ingress/egress
 - Passed between parser/MAU stages/deparser
- Packet occupancy vector (POV)
 - Bit vector indicating headers
 - Stored in PHV



Midend/backend tour

MidEnd:

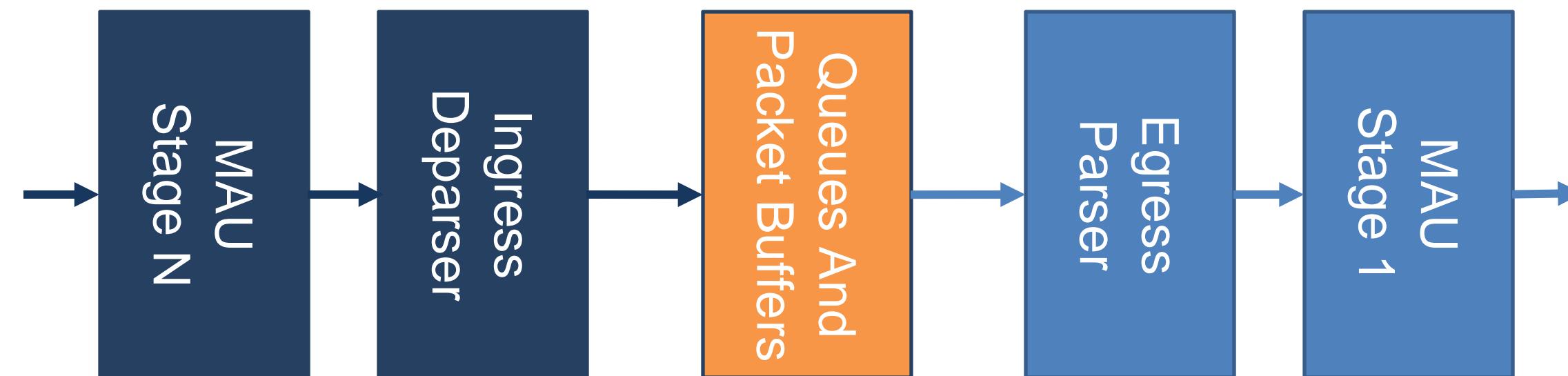
- Similarity to PsaSwitchMidEnd
- Some specializations (P4:: → BFN::)
- Design patterns: adherence + recommendations
- Architecture translation (TNA IR nodes)
- Normalization (tna/t2na/v1model)
- Simplifications (cast elimination, control rewrites, ...)
- Varbit: verify usage / desugar
- ...

```
addPasses(  
    new P4::RemoveMiss(),  
    new P4::EliminateNewtype(),  
    new P4::EliminateBitFields(),  
    new BFN::TypeChecking(),  
    new BFN::SetDefaultSize(), // set default table size for tables w/o "size"  
    new BFN::OrderTables(),  
    new BFN::OrderArguments(),  
    new BFN::OptionalTertiaryMatchTypeConverter(),  
    new BFN::ArchTranslation(),  
    new BFN::FindArchitecture(),  
    new BFN::CheckBitFields(),  
    new BFN::CheckDesignPattern(), // add checks for p4 design pattern here.  
    new BFN::SetDefaultSize(), // belt and suspenders, in case of IR mutation  
    new BFN::InitializeTableSelect(),  
    new BFN::InitializeTableEngine(),  
    new EnumOn32bits::FindStateInEnumOutputs(),  
    new P4::ConvertEnums(),  
    new P4::ConstantFolding(),  
    new P4::SimplifyBitFields(),  
    new P4::SimplifyControlFlow(),  
    new P4::SimplifyKey(&refMap, &typeMap,  
        BFN::KeyIsSimple::getPolicy()),  
    DeviceTypeConversion::convertToTDFIMO || options.disable_direct_exit ?  
        new P4::RemoveExports() : nullptr,  
    new BFN::ConstantFolding(),  
    new BFN::ElimCasts(),  
    new BFN::ReplaceTableSelection(),  
    new BFN::TypeChecking(),  
    // has to be early enough for setValid to still not be lowered  
    new BFN::CheckVarbitAccess(),  
    new BFN::MoveBitFields(),  
    new BFN::SimplifySelectCases(), // require constant keysets  
    new BFN::ExpandLookahead(),  
    new P4::ExpandDepth(),  
    new P4::SimplifyBitFields(),  
    new P4::ReplaceSelectRange(),  
    new P4::StrengthReduction(),  
    new BFN::CopyHeader(),  
    new BFN::SimplifyComparisons(),  
    new BFN::CopyHeader() // must run after copy structure  
    new P4::SimplifyStatement(),  
    new BFN::LocalCopyPropagation(),  
    new P4::SimplifyArgs(),  
    new P4::NestedStructs(),  
    new P4::SimplifySelectList(),  
    new BFN::SimplifySelectList(),  
  
    new P4::Predication(),  
    new P4::MoveDeclarations(), // more may have been introduced  
    new P4::ConstantFolding(),  
    new P4::SimplifyBitFields(),  
    new P4::LocalCopyPropagation(),  
    new P4::StrengthReduction(),  
    new P4::MoveDeclarations(),  
    new NormalizedHashTable(),  
    new P4::SimplifyNestedIf(),  
  
    new P4::SimplifyControlFlow(),  
    new CompilerTimeOperations(),  
    new P4::TableHit(),  
  
    evaluator,  
    new VisitFunction() -> const IR::Node * {  
        auto topLevel = evaluator->getTopLevelBlock();  
        auto main = topLevel->getMain();  
        if (!main)  
            // nothing further to do  
            return nullptr;  
        for (IR::Block::iterator i = main->begin(); i != main->end(); ++i)  
            if (i->getDeclByName())  
                continue;  
            if (!i)  
                skip_controls->emplace();  
        return root;  
    },  
    new P4::SynthesizeActions(&refMap, &typeMap,  
        new ActionSynthesisPolicy()),  
    new P4::MoveActionsToTables(),  
    new BFN::CopyBlockPragmas(),  
    () {  
        new RewriteEgressIntrinsicMetadataHeader() : nullptr,  
        new DesugarVarbitExtract(),  
        new RegisterReadCommon(),  
        new PingPongGeneration(),  
        new RegisterReadWrite(),  
        new BFN::AnnotateWithInHash(),  
        new BFN::CopyBitFields(),  
        BackendOptions().disable_parse_min_depth_limit &  
            ? nullptr  
            : new BFN::ParserEnforceDepthReq(),  
        // Collects source info for logging. Call this after all transformations are complete.  
        sourceInfoLogging.  
    }  
);
```

Midend/backend tour (cont.)

BridgedPacking:

- Runs between MidEnd and BackEnd
- Packs “bridged” metadata
 - Ingress → egress metadata
 - Prepended to packet



- Translation to backend IR nodes (MidEnd only introduces subset)

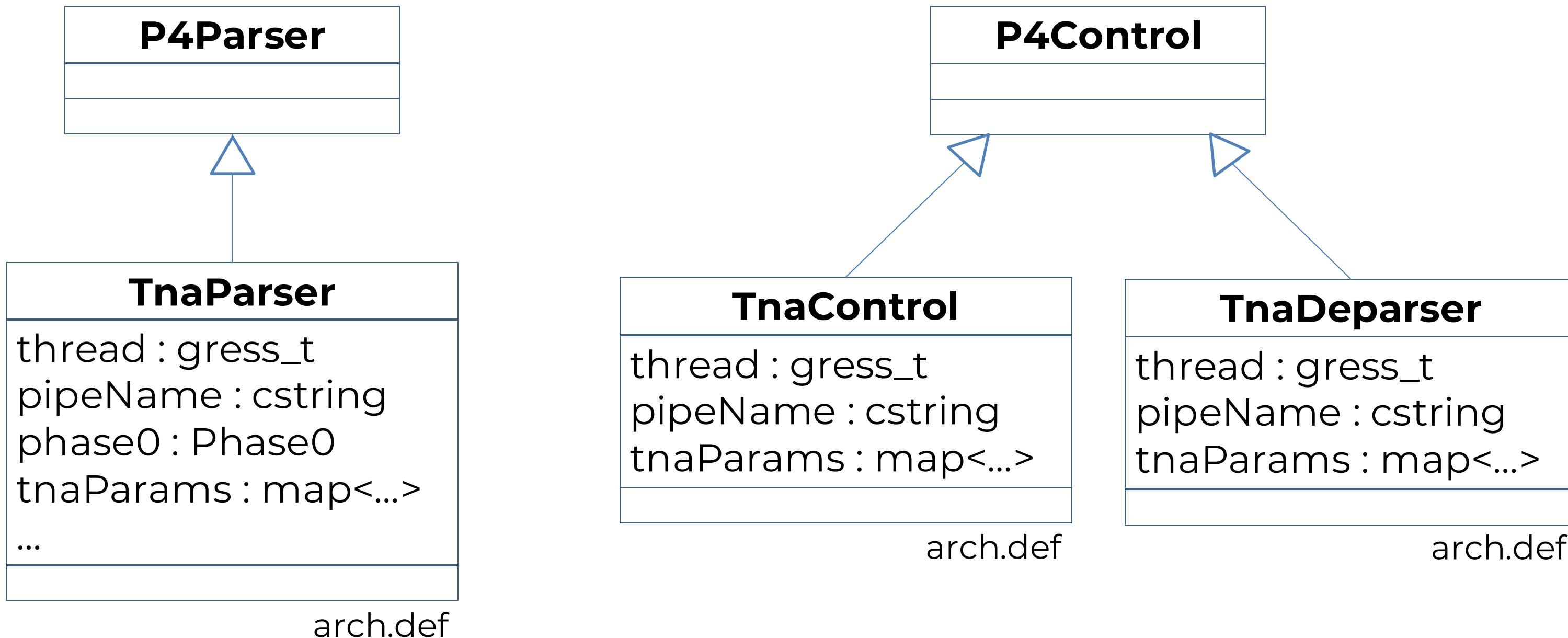
Midend/backend tour (cont.)

BackEnd:

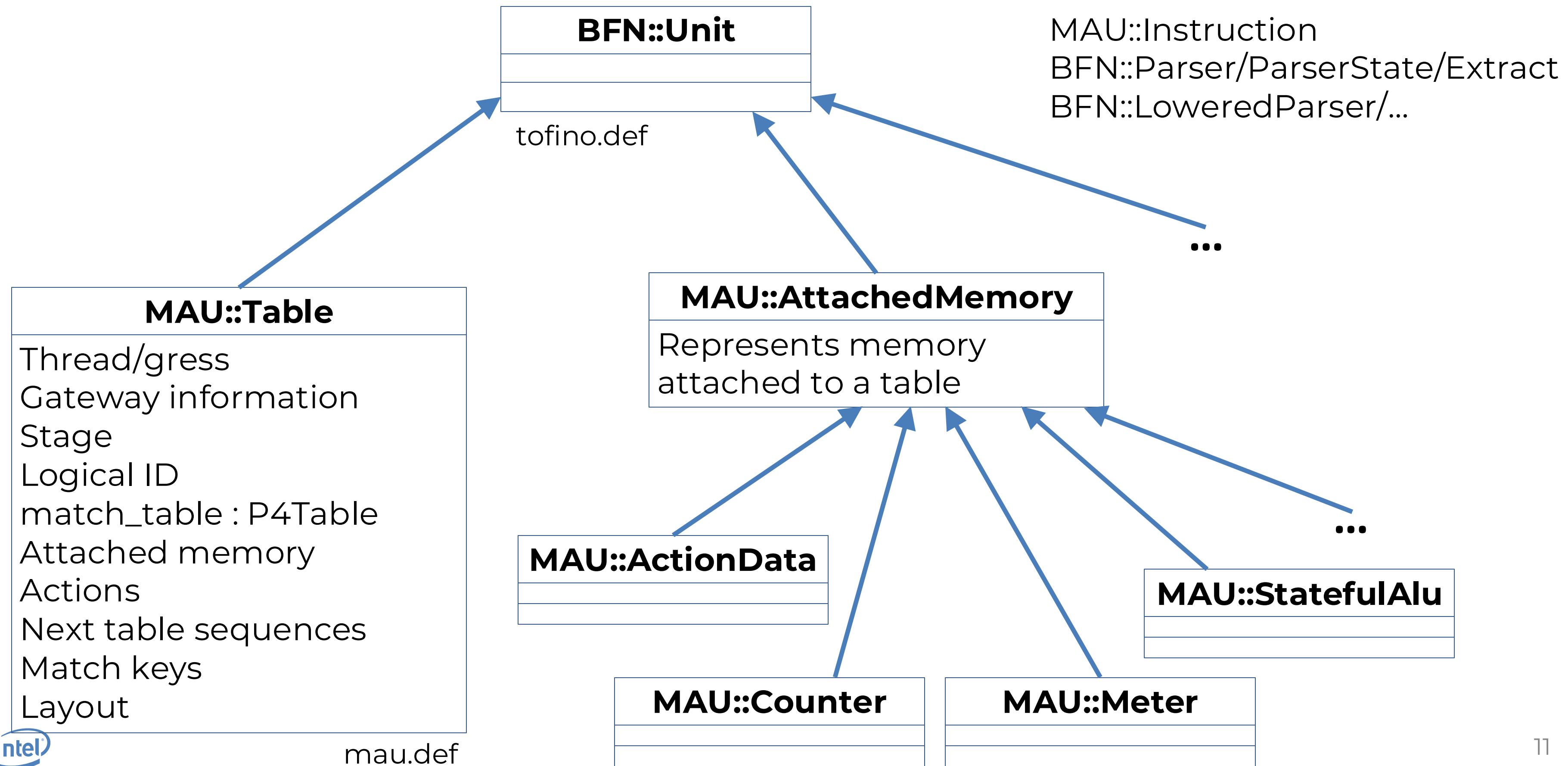
- Instruction selection
- PHV allocation
- Table allocation
- Smaller features:
 - Aliasing (detecting two fields are equivalent → share allocation)
 - Metadata initialization (optional)
 - Pragma collection/application
 - Parser IR lowering
 - ...

Tofino IR nodes

- Custom Tofino IR nodes replace some open-source IR nodes
- Reason: better represent underlying hardware



Tofino IR nodes (cont.)



PhvInfo + PHV::Field objects

PhvInfo

- Information for PHV-backed storage (fields + metadata)
- Iterators
- Query interface (e.g., field(), bits_allocated(), ...)
- Populated by CollectPhvInfo pass

PHV::Field

- Basic info for a field (name, ID, size, offset within header, properties, ...)
- Alignment constraints
- PHV container allocation (if any)
- Alias information
- Higher-order functions to iterate over and process allocations

Resource allocation

Classic:



Alt-PHV:



PHV alloc

```
collect_constraints();  
vector<Cluster> clusters = create_clusters();  
  
for (auto cluster : clusters) {  
    for (auto container_group : container_groups) {  
        for (auto slice : cluster) {  
            vector<...> possible_allocation = try_alloc(slice, container_group);  
            if (possible_allocation.size() == 0)  
                break;  
            Allocation best_allocation = best_allocation(possible_allocation);  
            place_slice(best_allocation);  
        } } }
```

PHV partitioned into groups
MAU instruction:

- Operands + target field: same group
- Operands: same alignment

```
if (unplaced_clusters())  
    ::error("Not all clusters placed");
```

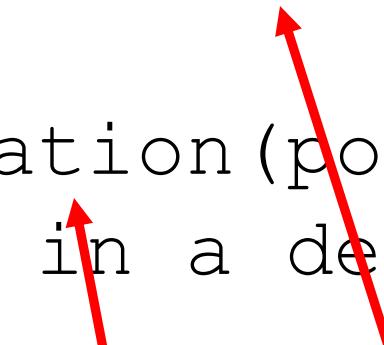
Try in each container at each valid alignment

Multiple tries before failing. Several different search/scoring strategies.

Resource allocation (cont.)

Table alloc

```
while (true) {  
    set<Table> possible_tables = placeable_tables_due_to_dependencies();  
    if (possible_tables.empty())  
        break;  
    vector<Allocation> possible_allocation;  
    for (possible_table : possible_tables) {  
        possible_allocation.push_back(find_allocation(possible_table));  
    }  
    Allocation best_allocation = best_allocation(possible_allocations);  
    place_table(best_allocation); // Locks in a decision  
}  
  
if (unplaced_tables())  
    ::error("Not all tables placed");
```



Prefer tables in longer sequences

Prefer larger tables

Pack into earlier stages

Actual process more complex. Does internal and external backtracking.

Backtracking

- Local within table placement:
 - Record partial placements
 - If table stage > max MAU stage:
 Return to earlier point and try different choice
 - Limit on backtrack attempts
- Global from table placement to PHV allocation:
 - Table placement info fed back to PHV alloc (via MauBacktrack object)
 - PHV alloc redone – uses backtrack info

Summary

- Tofino compiler will be open sourced soon
- Some custom IR nodes
- PhvInfo: collates information about fields/metadata, query iface
- PHV::Field: information about a single field/metadata
- PHV allocation / table allocation: iterative algorithms with retry
- Backtracking: used extensively in allocation to reach a solution

Acknowledgements

Huge team effort

Thank you to all who have contributed



Thank You