Deliberately Congesting a Switch for Better Network Functions Performance

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Network Functions Are Pervasive

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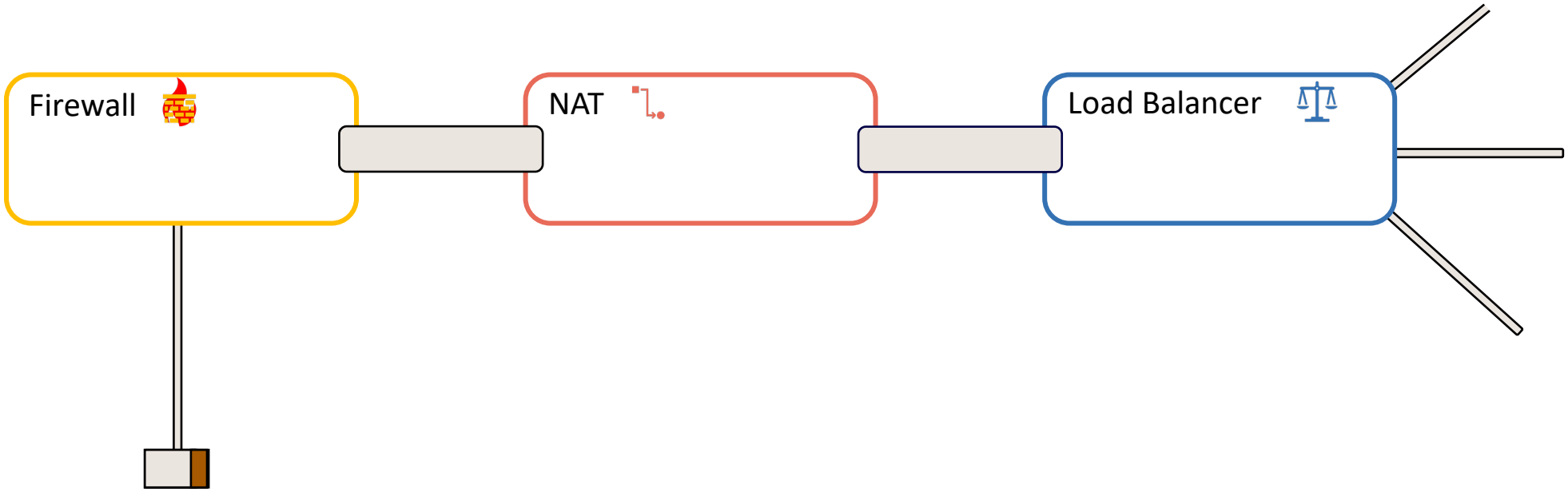
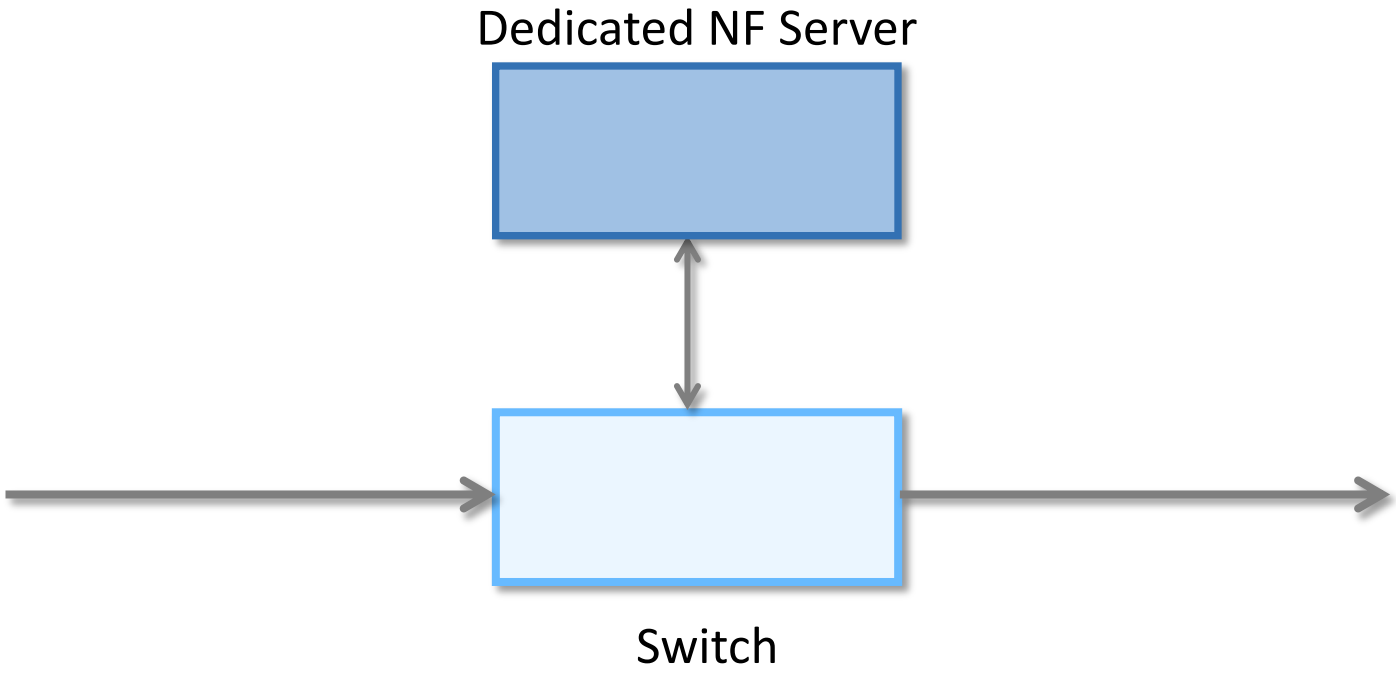
Network Functions Virtualization is an essential architectural paradigm of today's networks



Advanced NF Deployments



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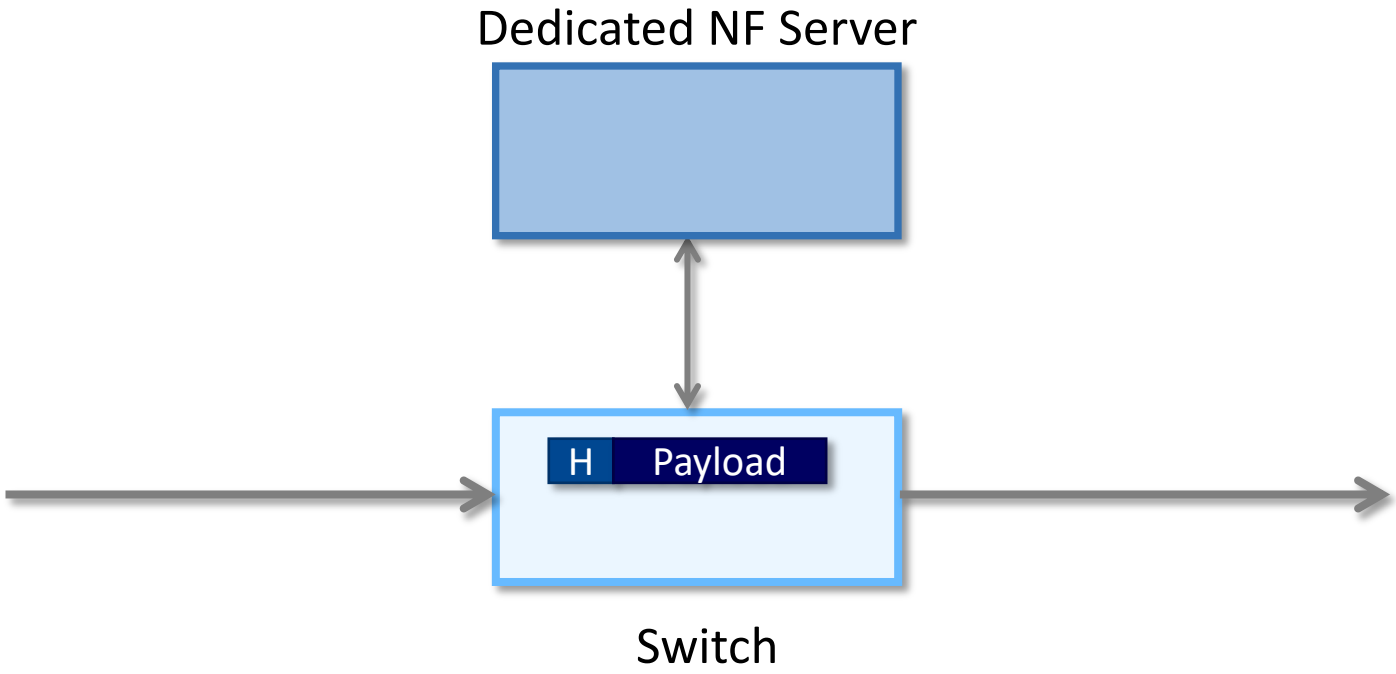

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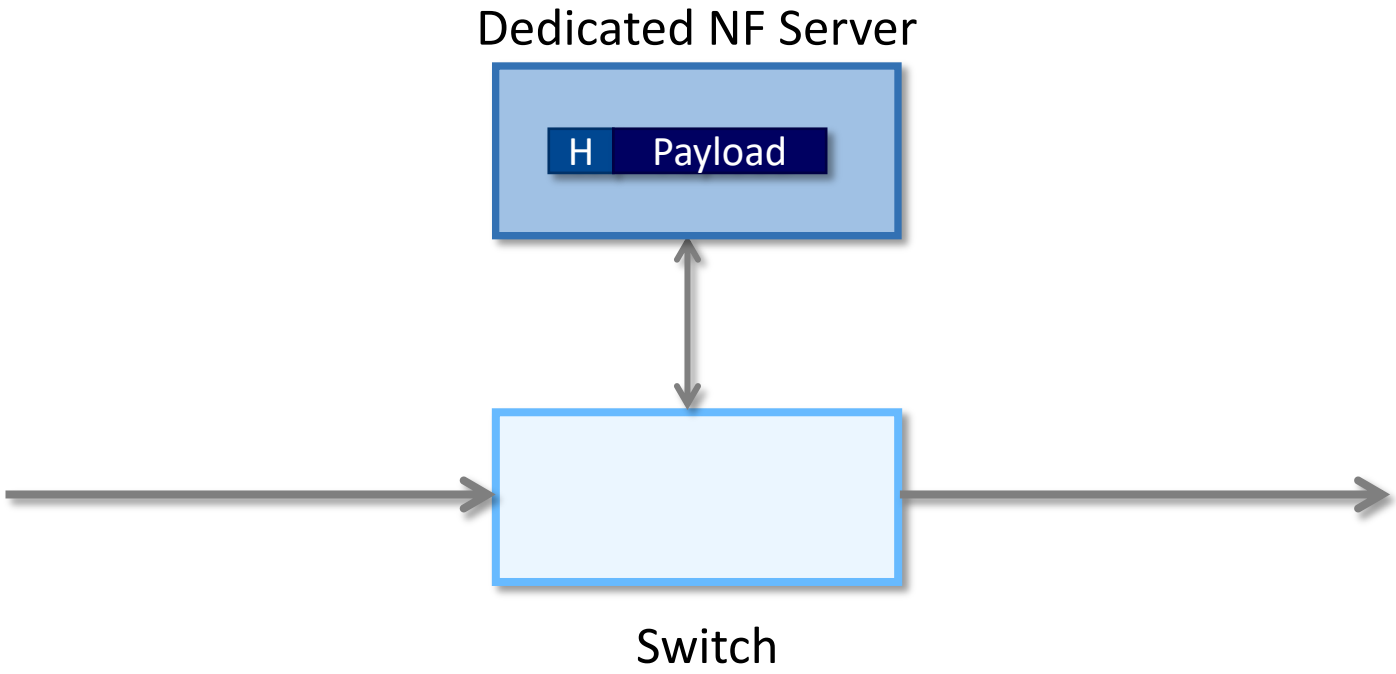
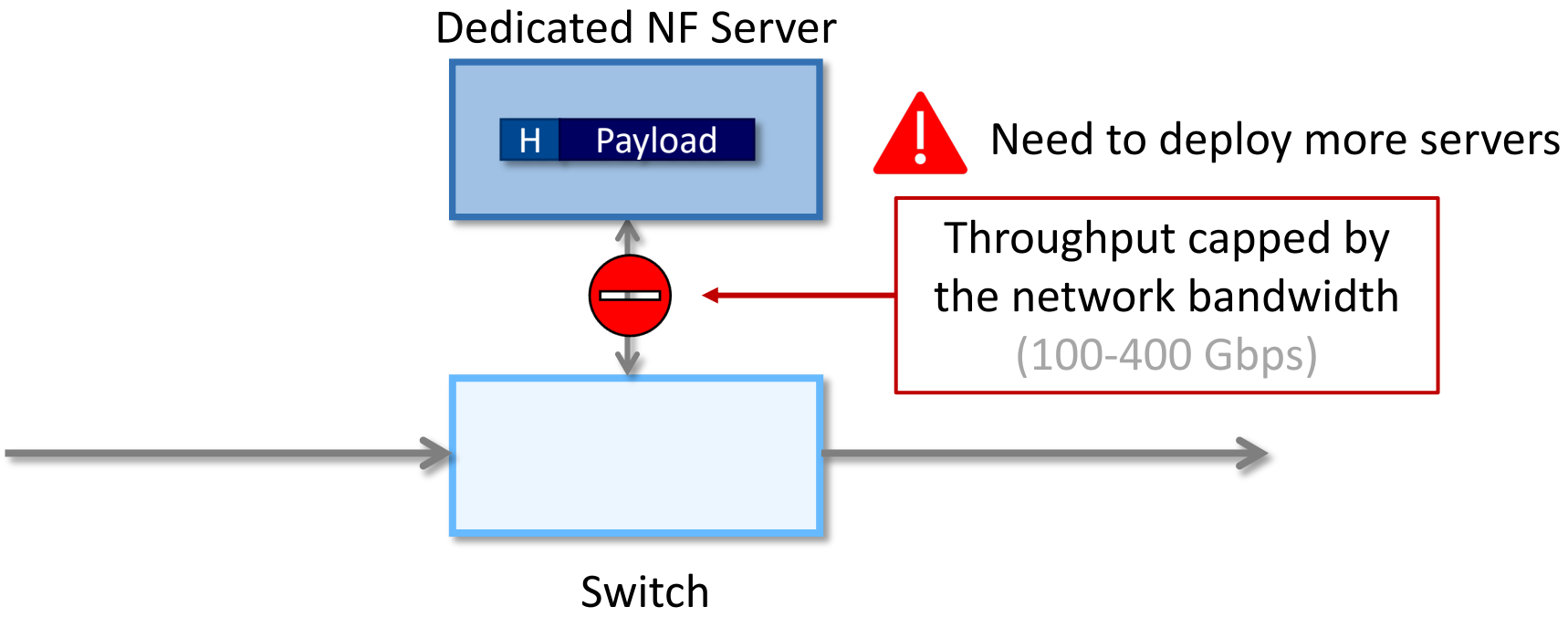


The Bandwidth Limit of Advanced NF Deployments



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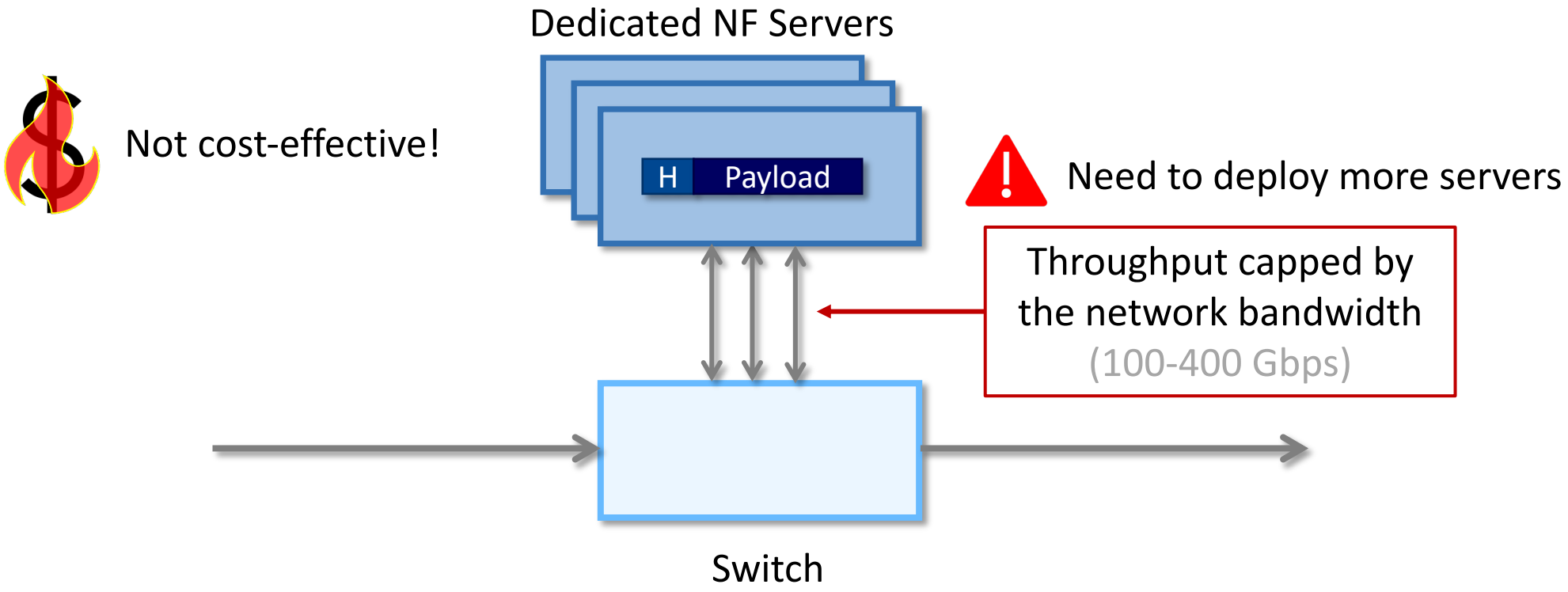
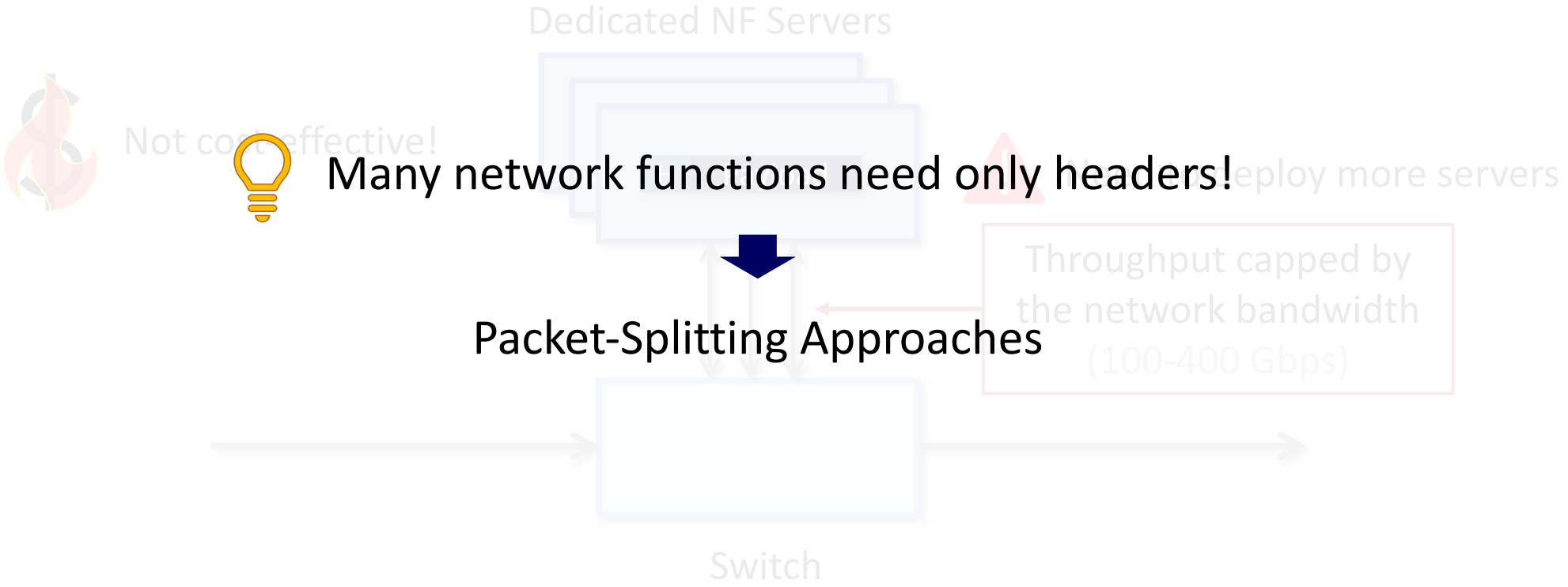


The Bandwidth Limit of Traditional NF Deployments



Packet-Splitting Approaches

State-of-the-art packet-splitting solutions increase NFs throughput

Improve NF Performance

Better CPU cache exploitation

Free up Bandwidth

Reduce the number of dedicated NF servers

Lower energy consumption

Complex Deployment

Require end-host modifications

Require available shared resources

Packet-Splitting Approaches

State-of-the-art packet-splitting solutions increase NFs throughput

Storing Payloads in the On-NIC Memory (nicmem) 

Storing Payloads on Shared Resources (Ribosome) 

Storing a Few Bytes in ASIC SRAM (PayloadPark) 

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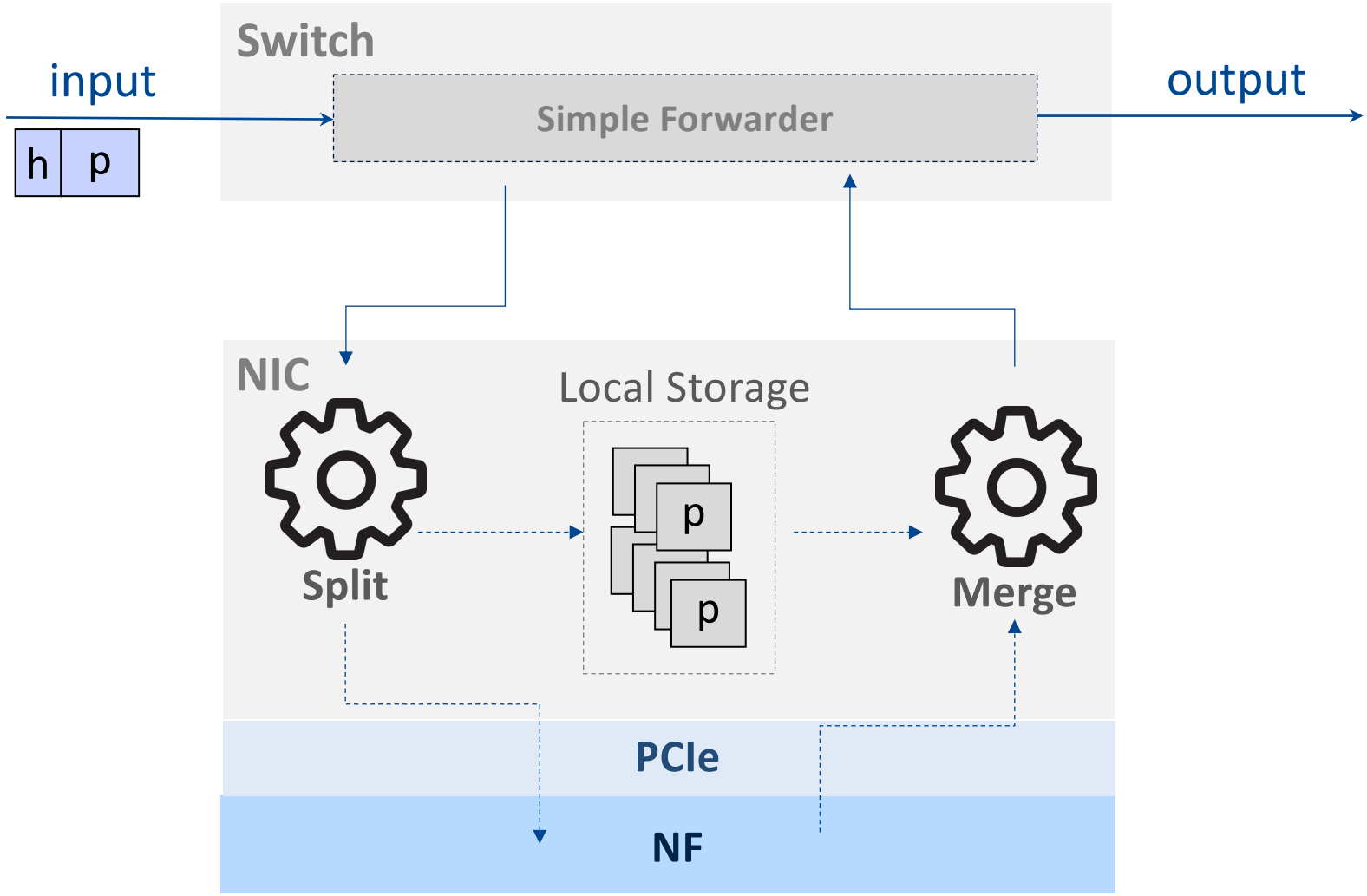

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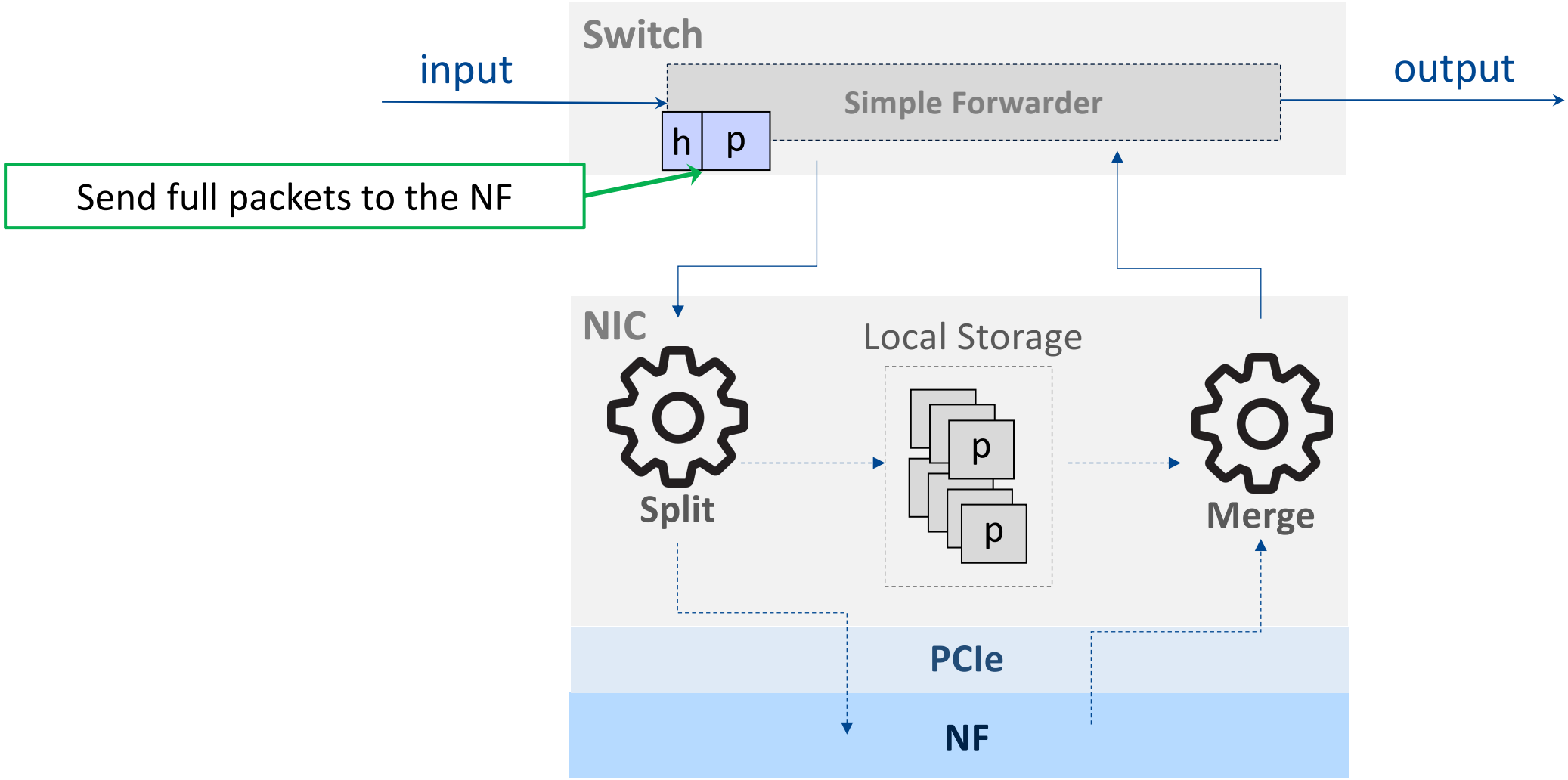

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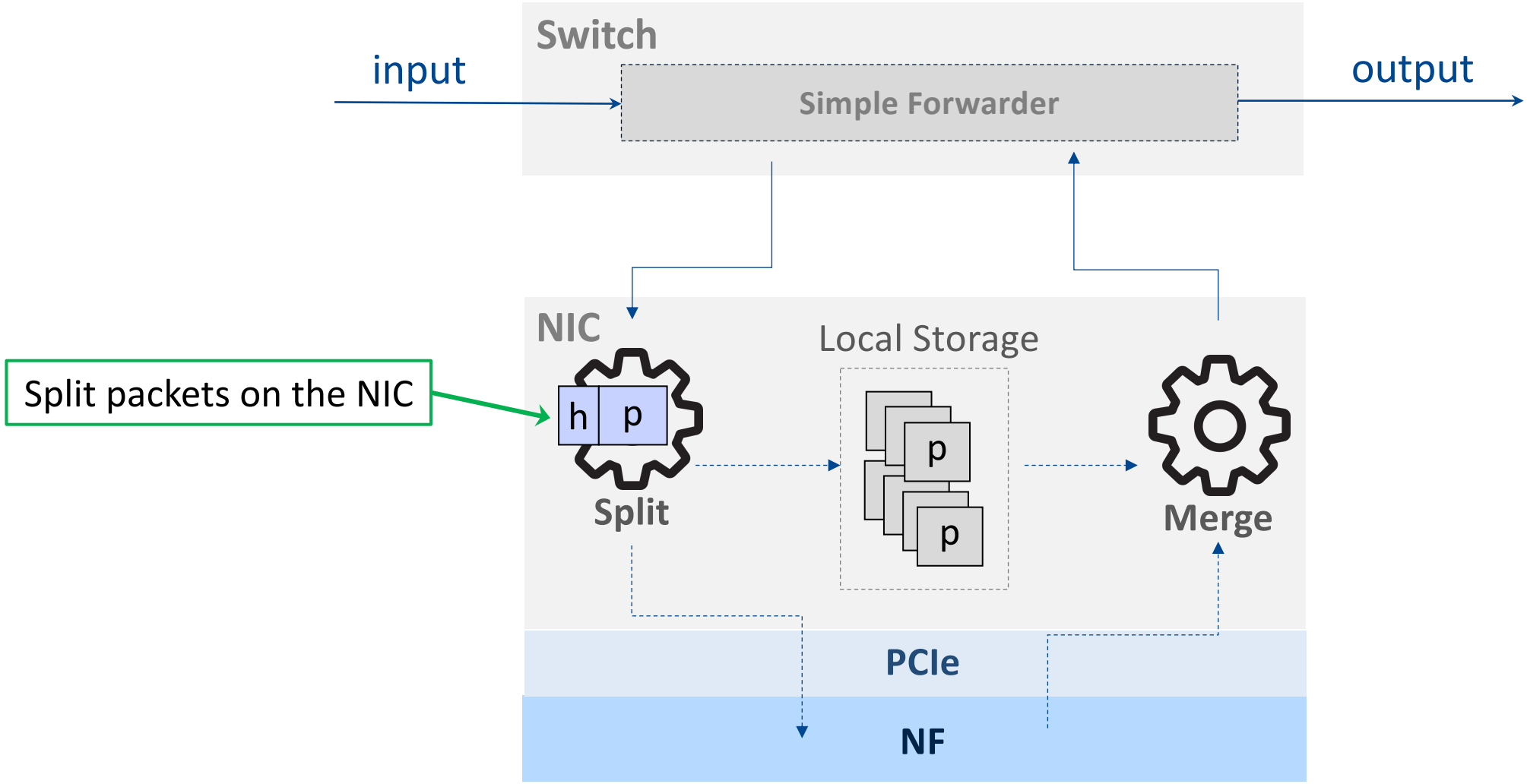

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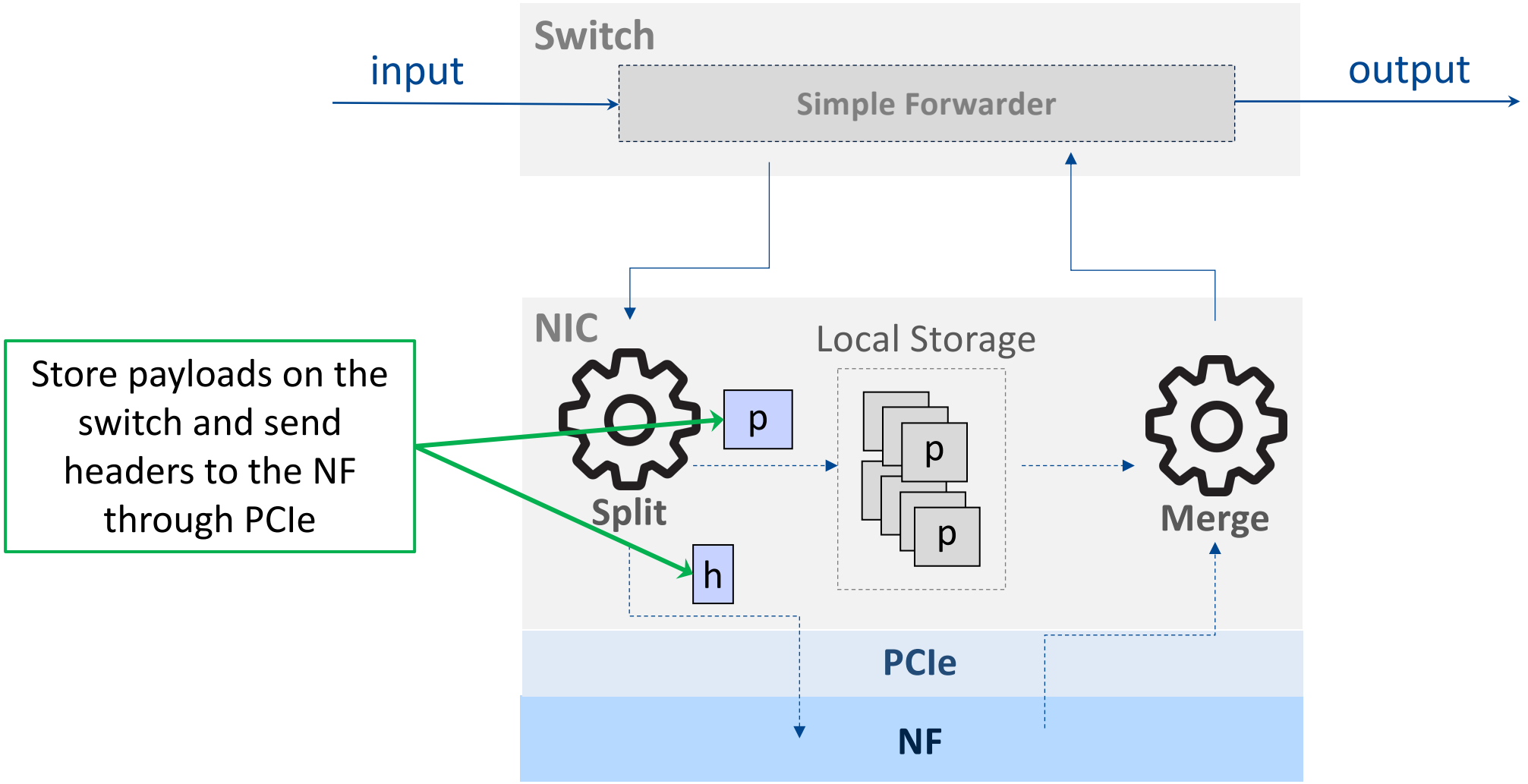

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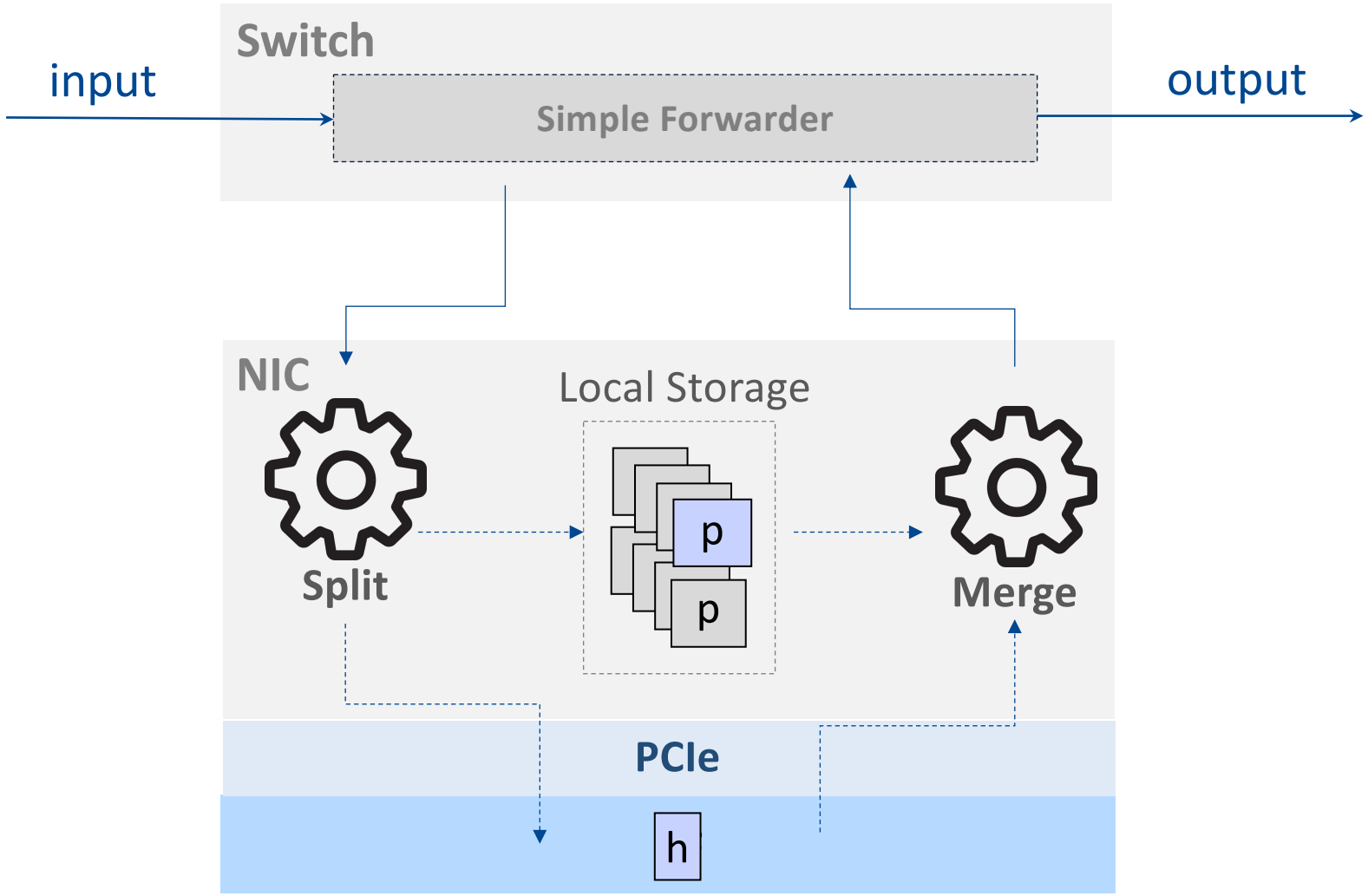

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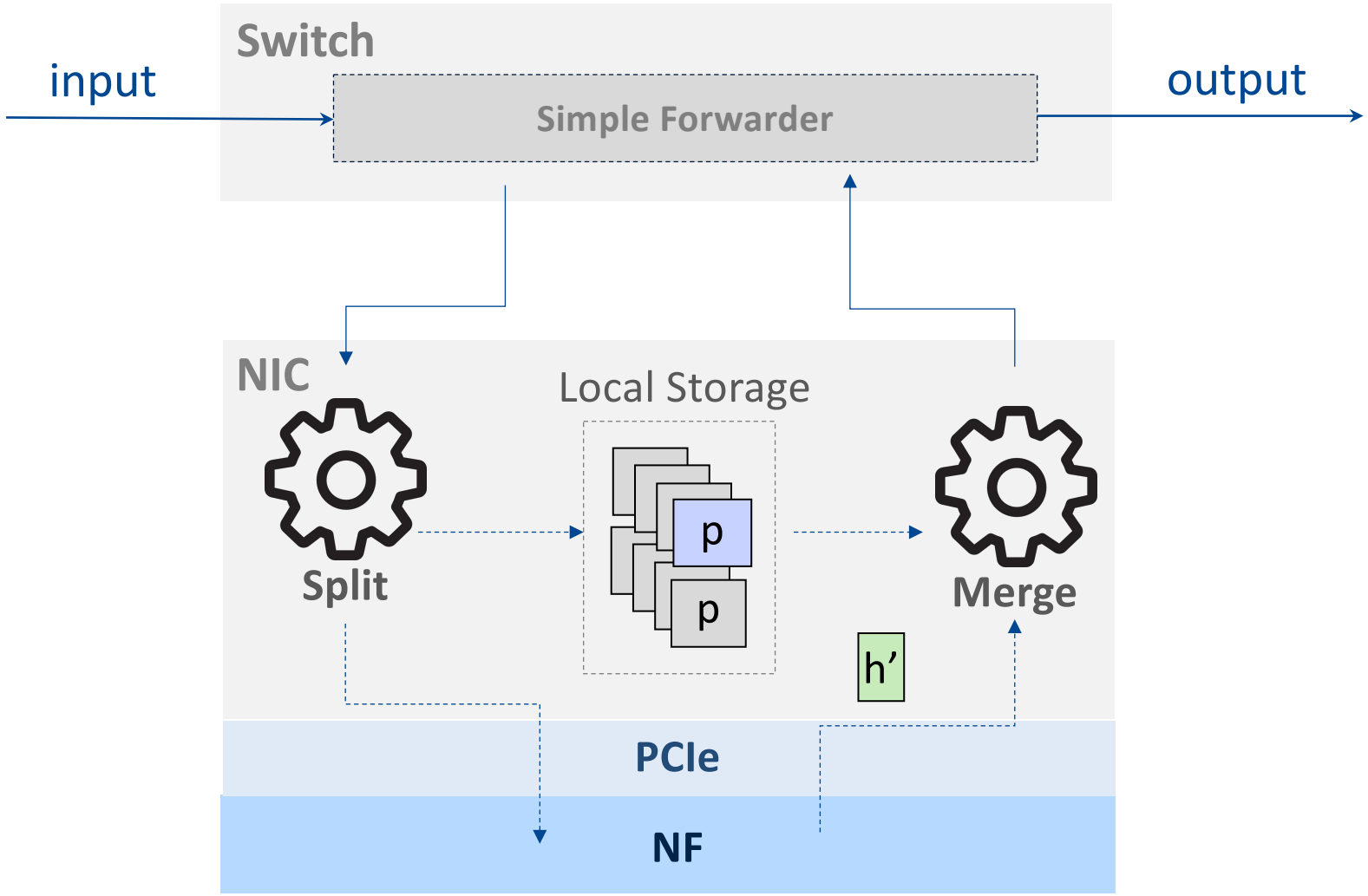

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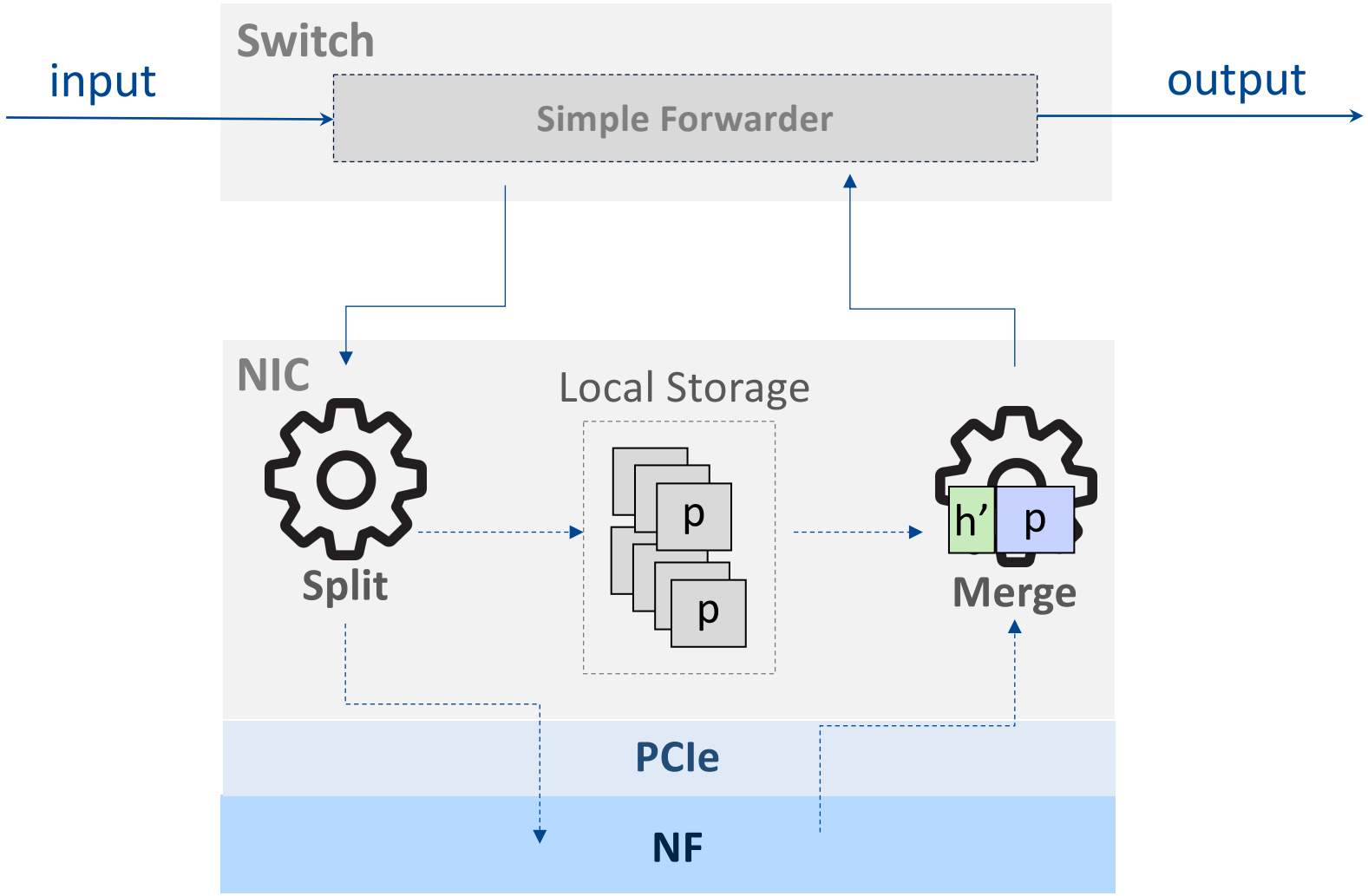

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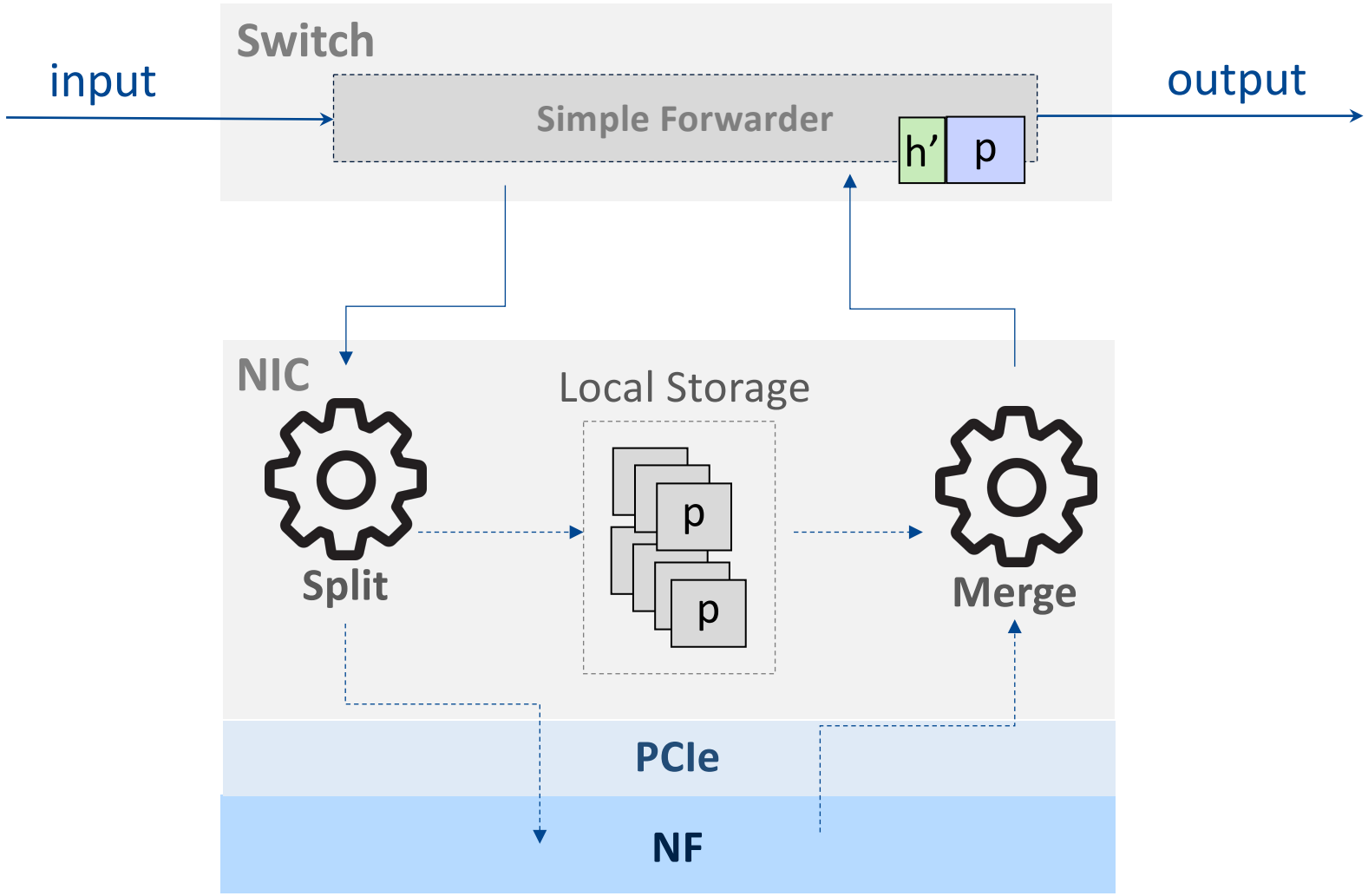

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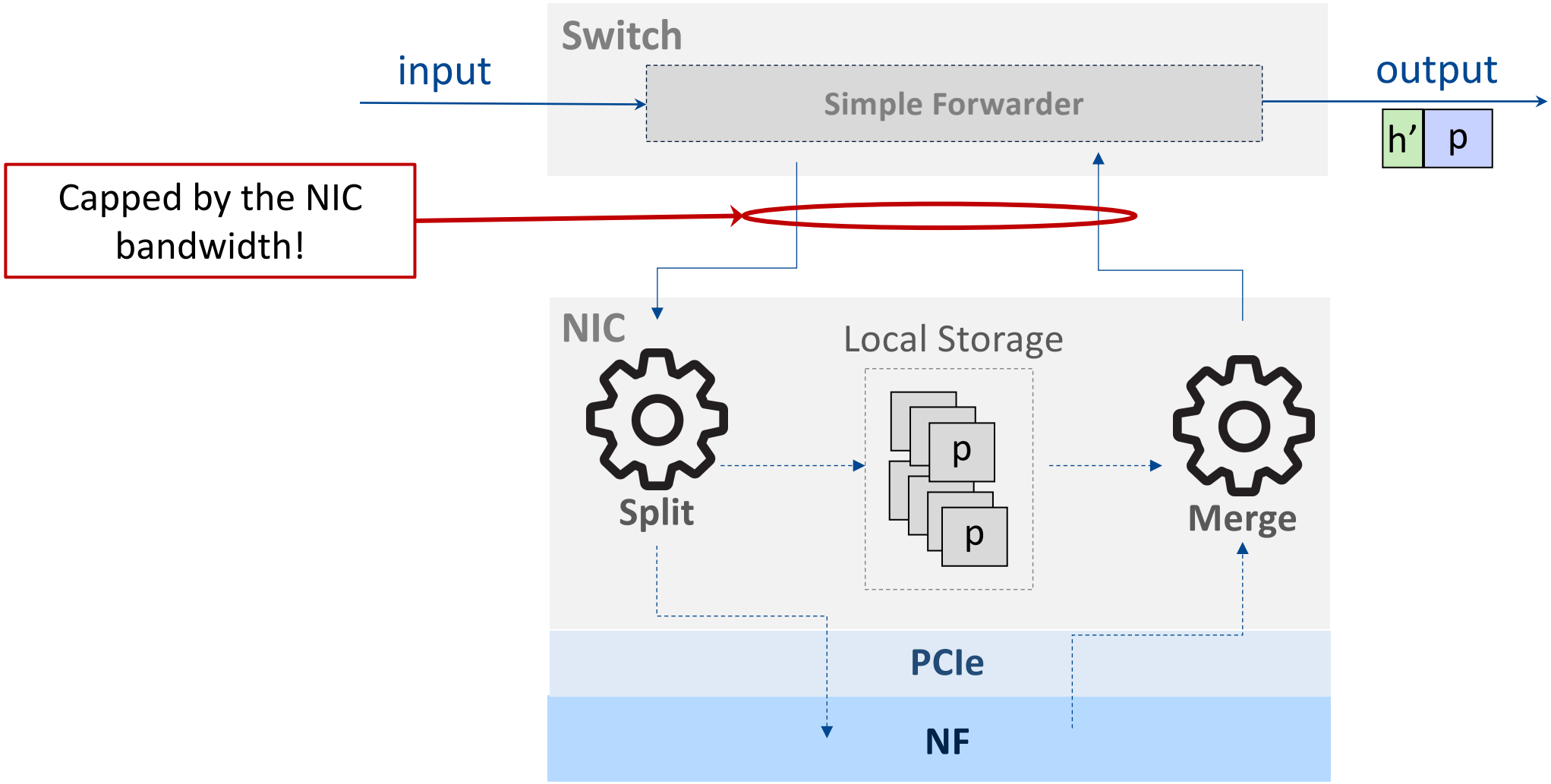

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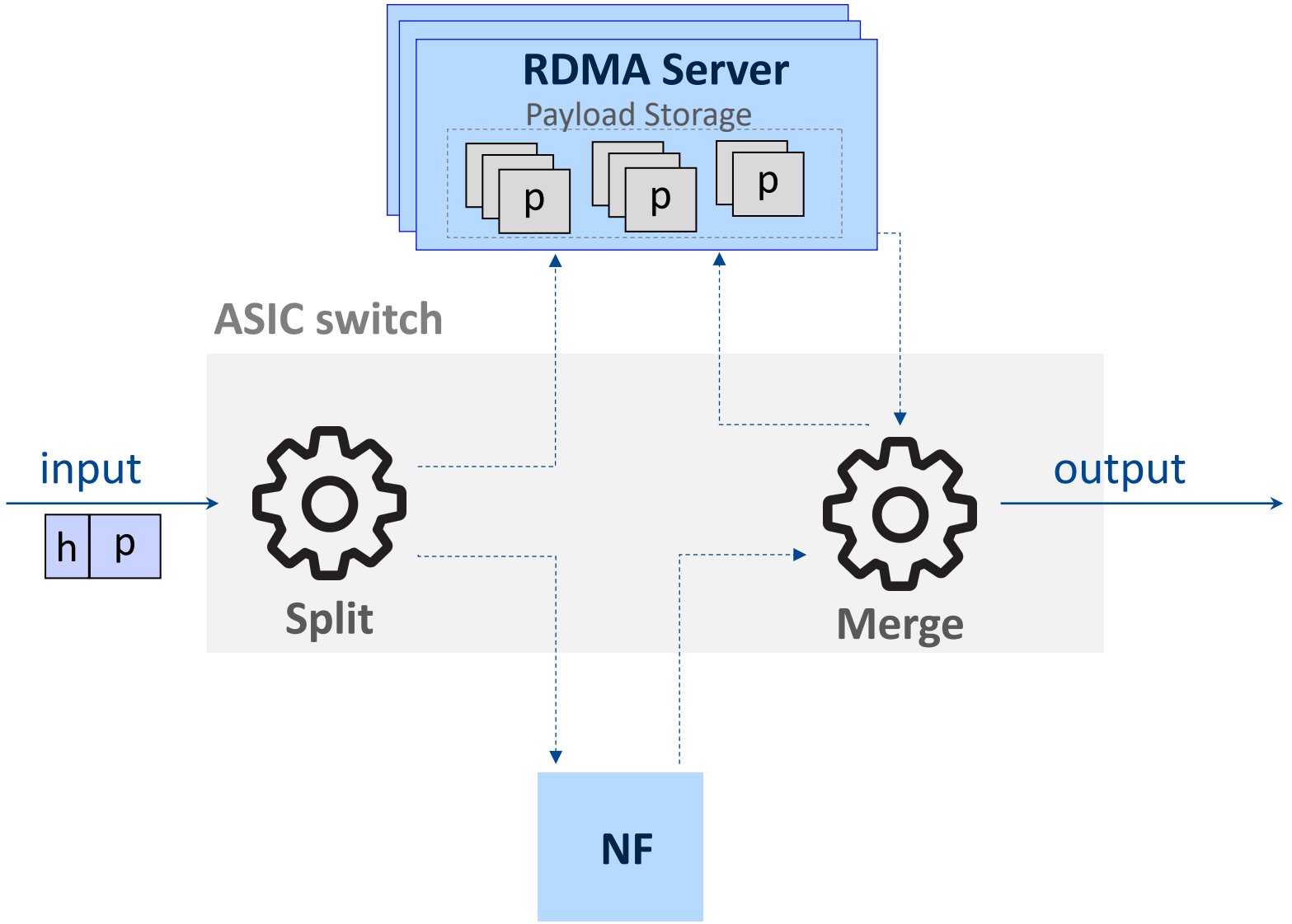

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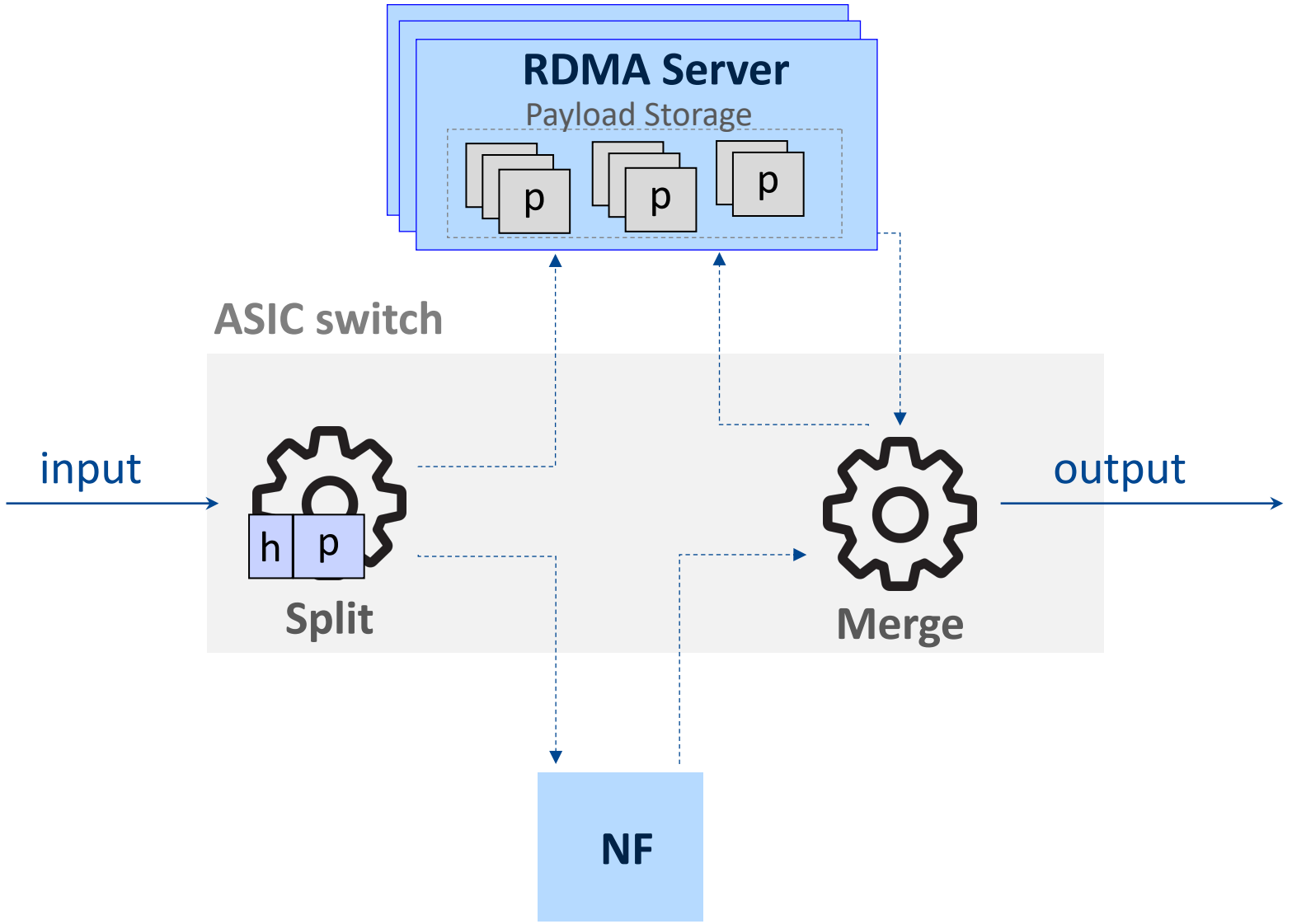

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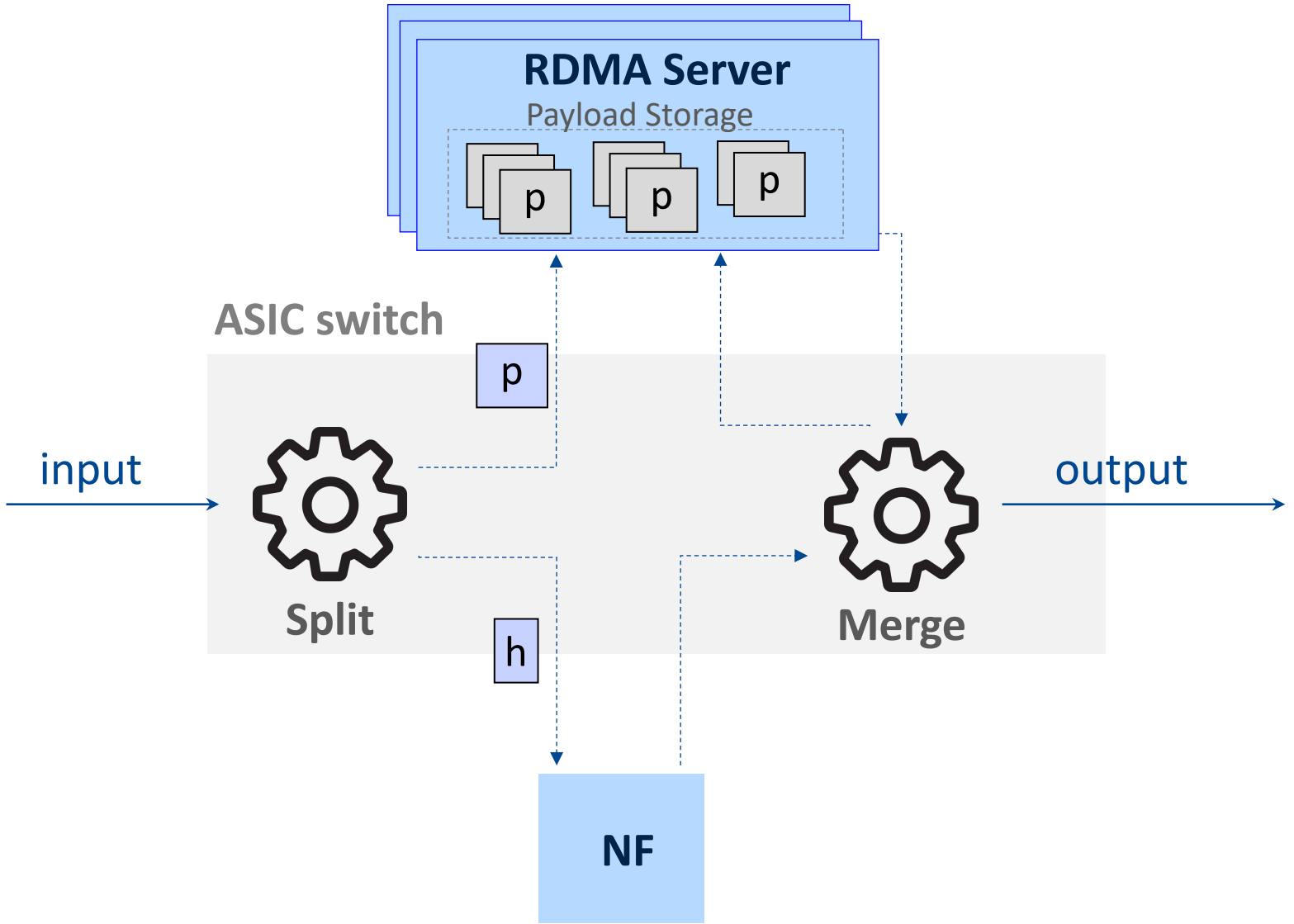

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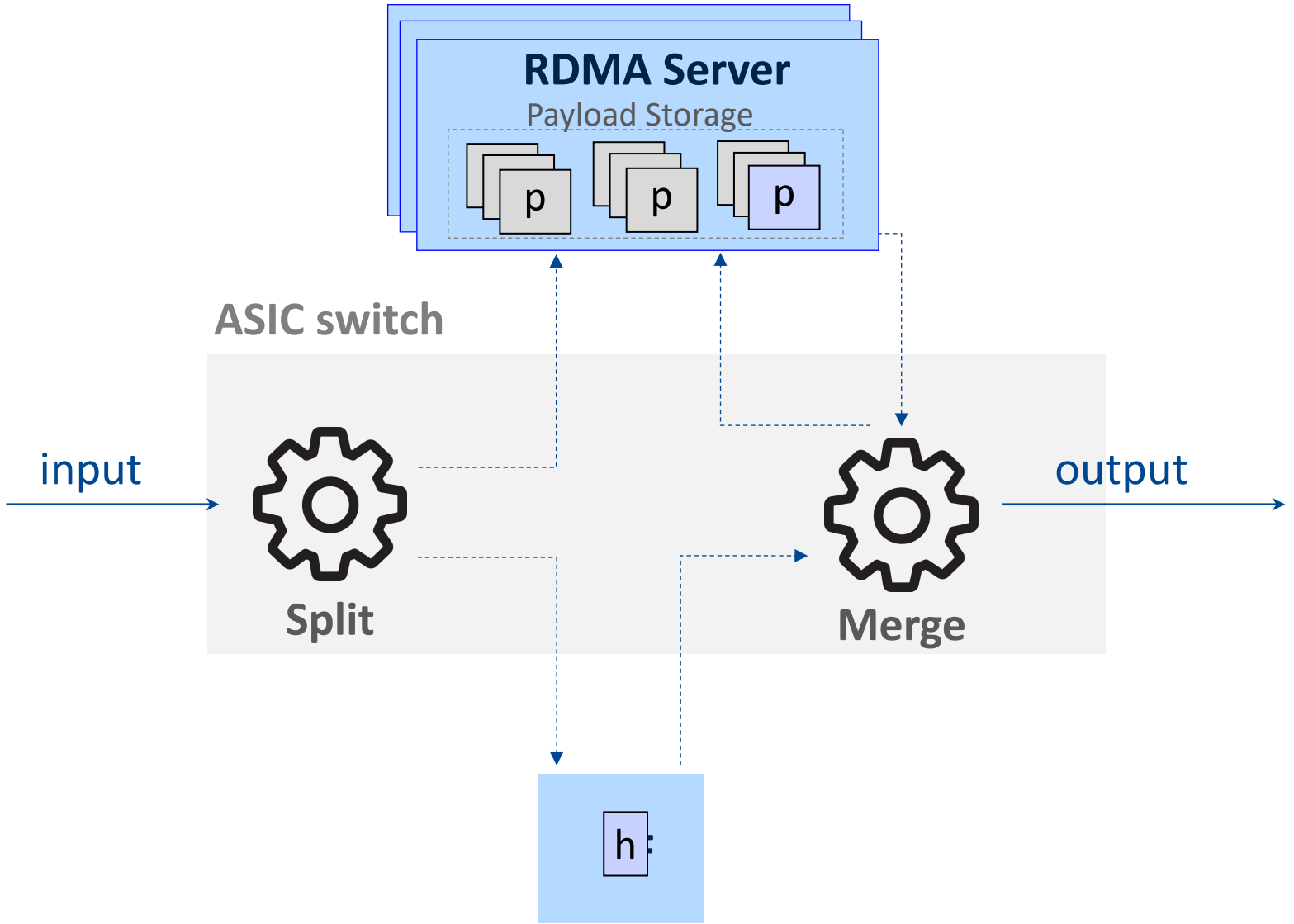

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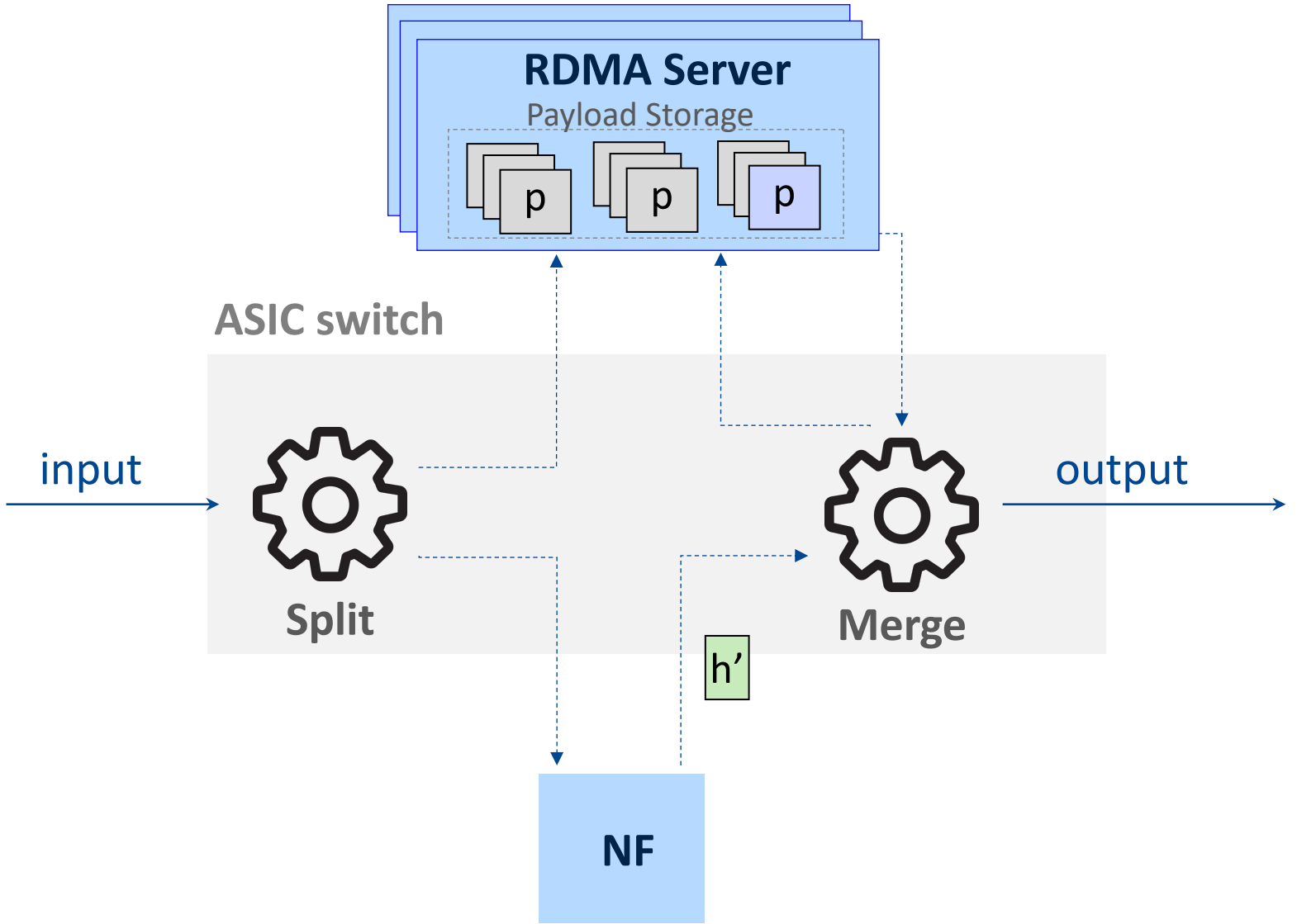

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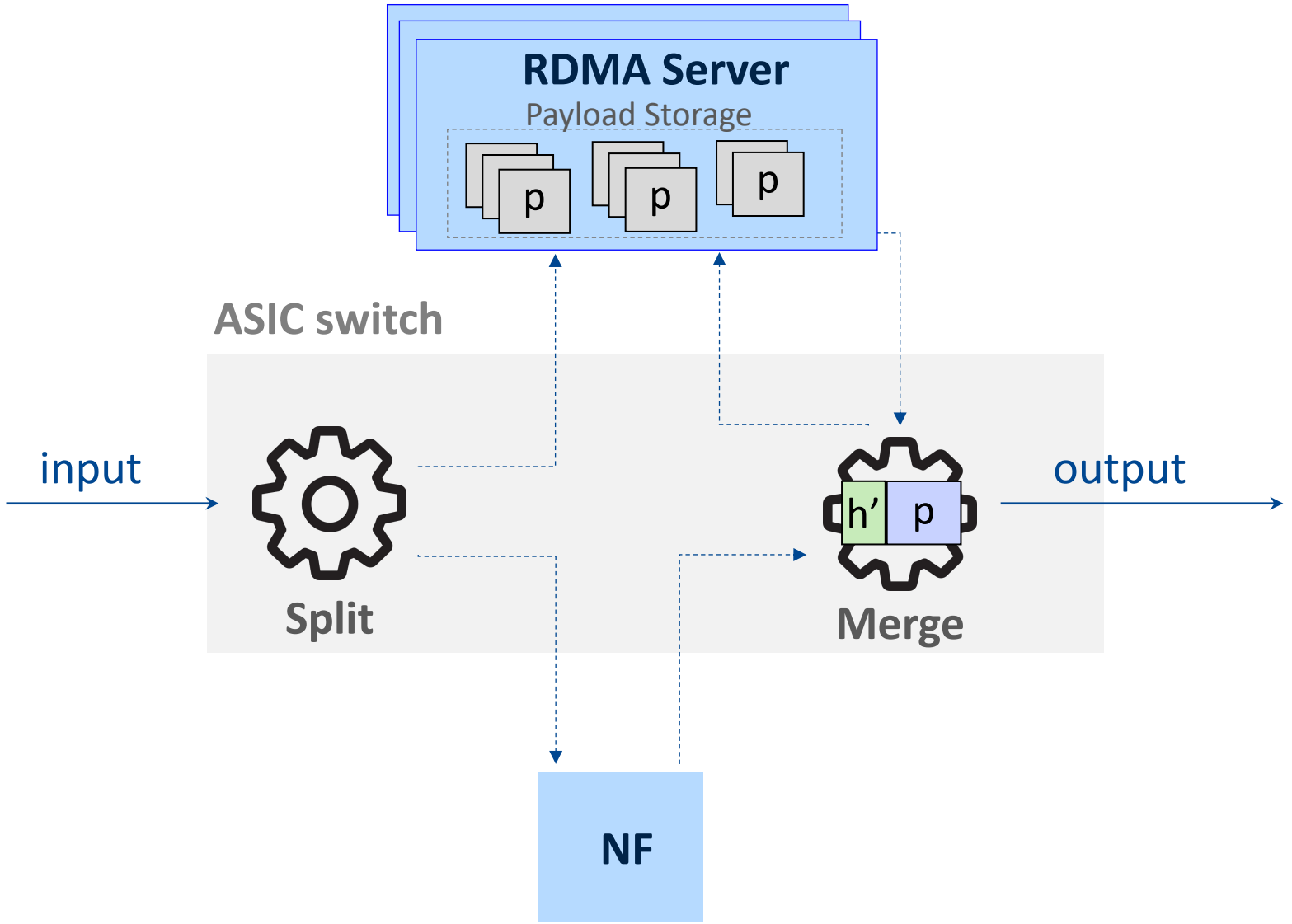
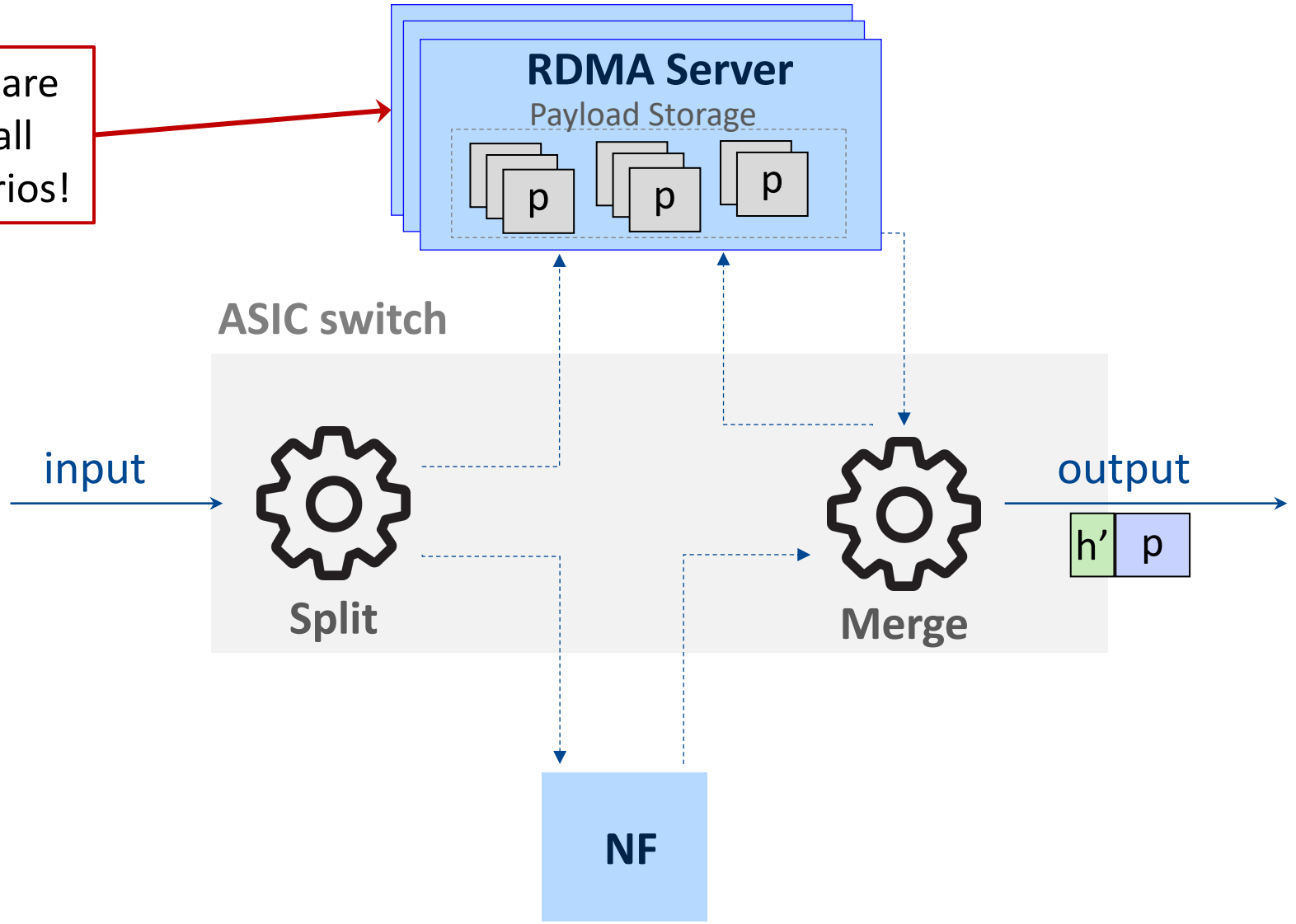
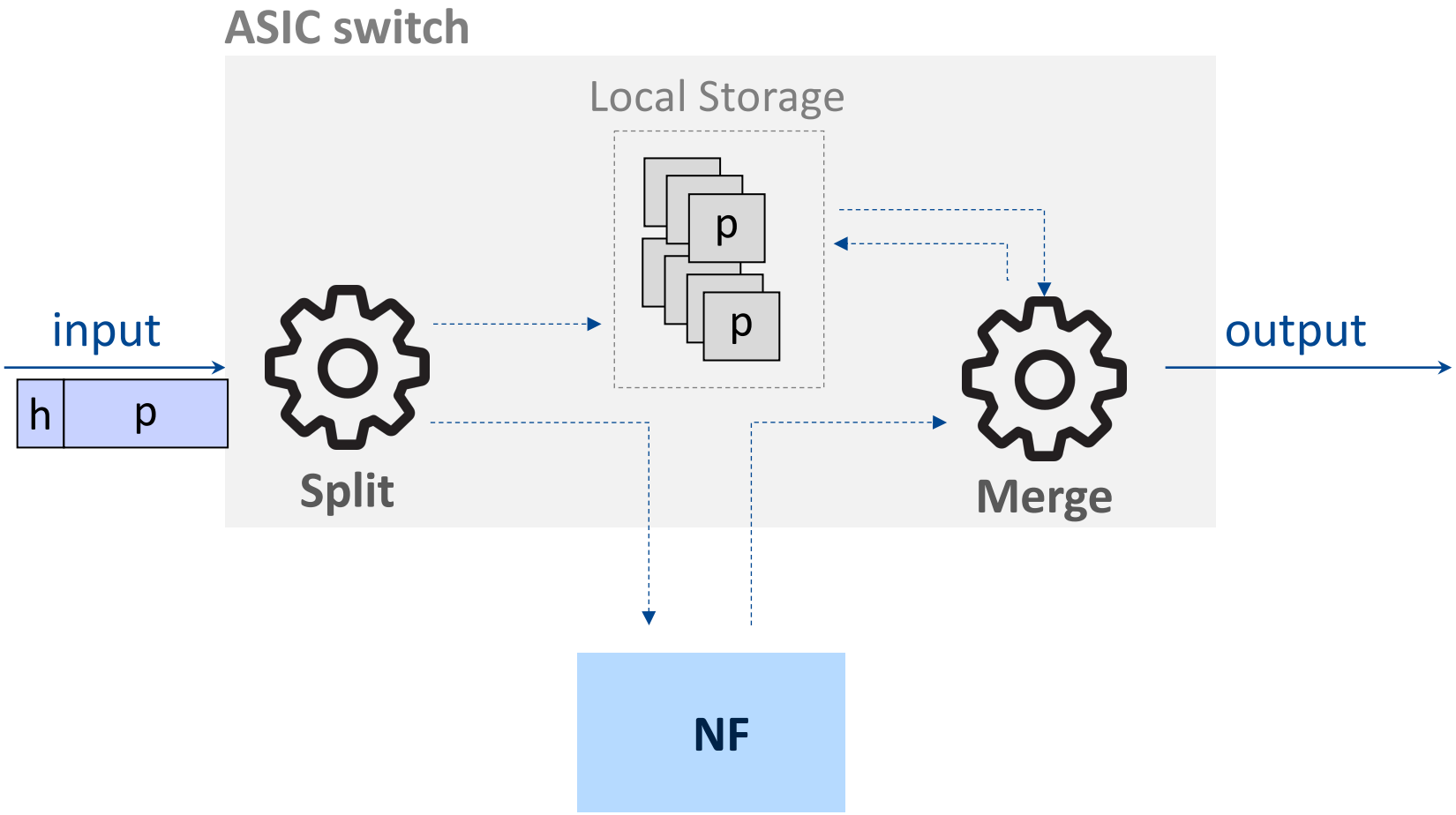


Storing Payloads on Shared Resources (Ribosome)

Shared resources are not available in all operational scenarios!



Storing a Few Bytes in ASIC SRAM (PayloadPark)



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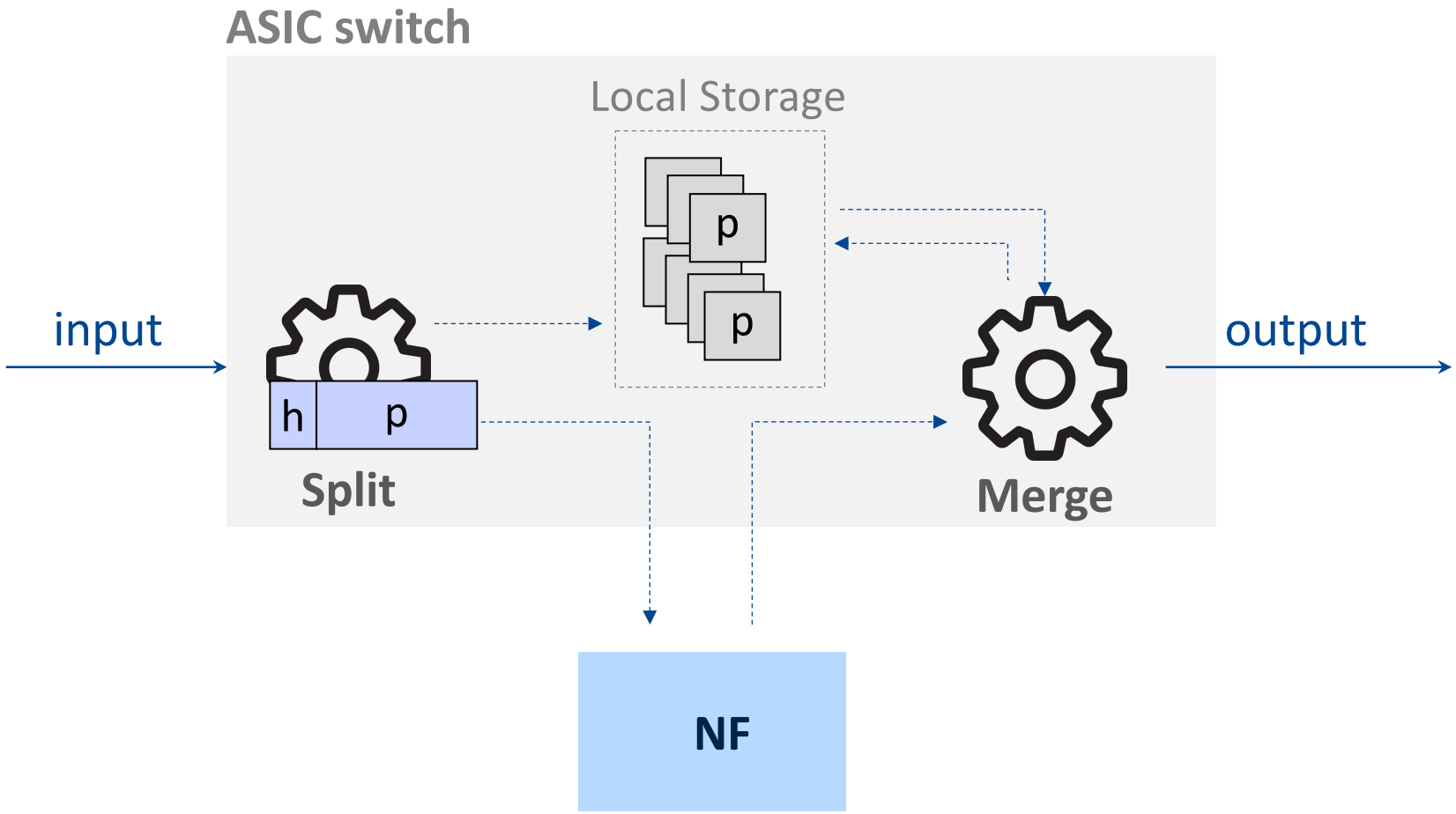

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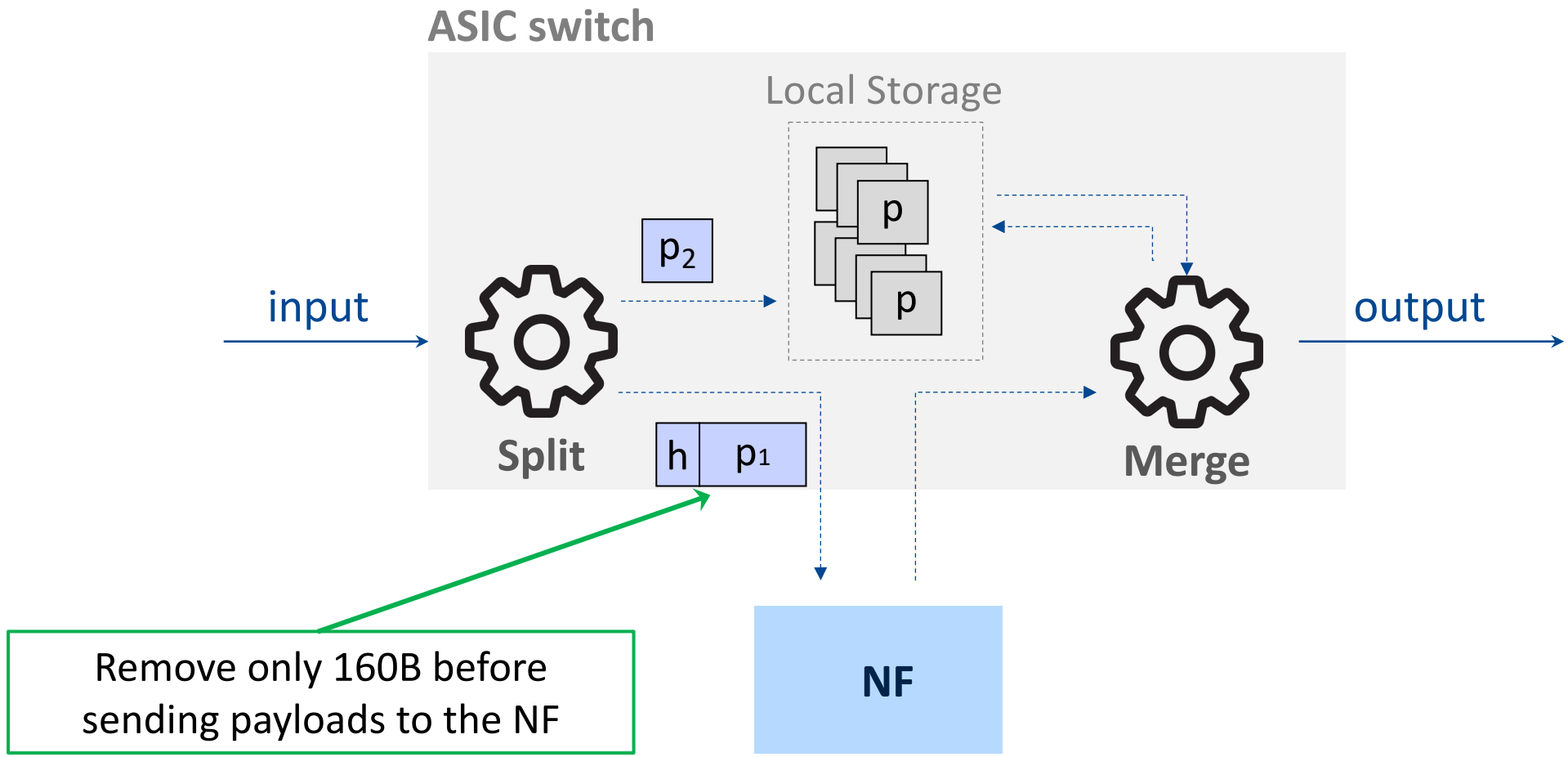

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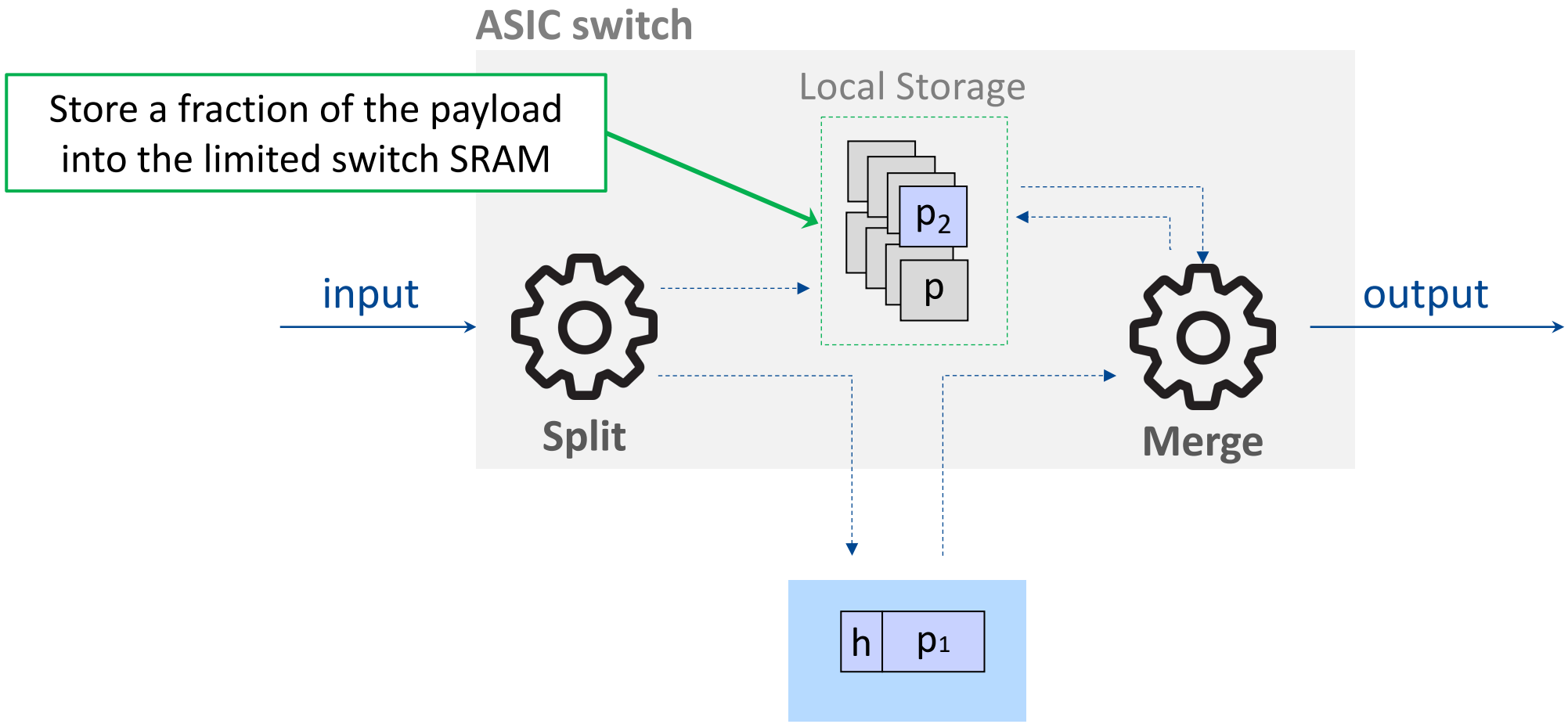

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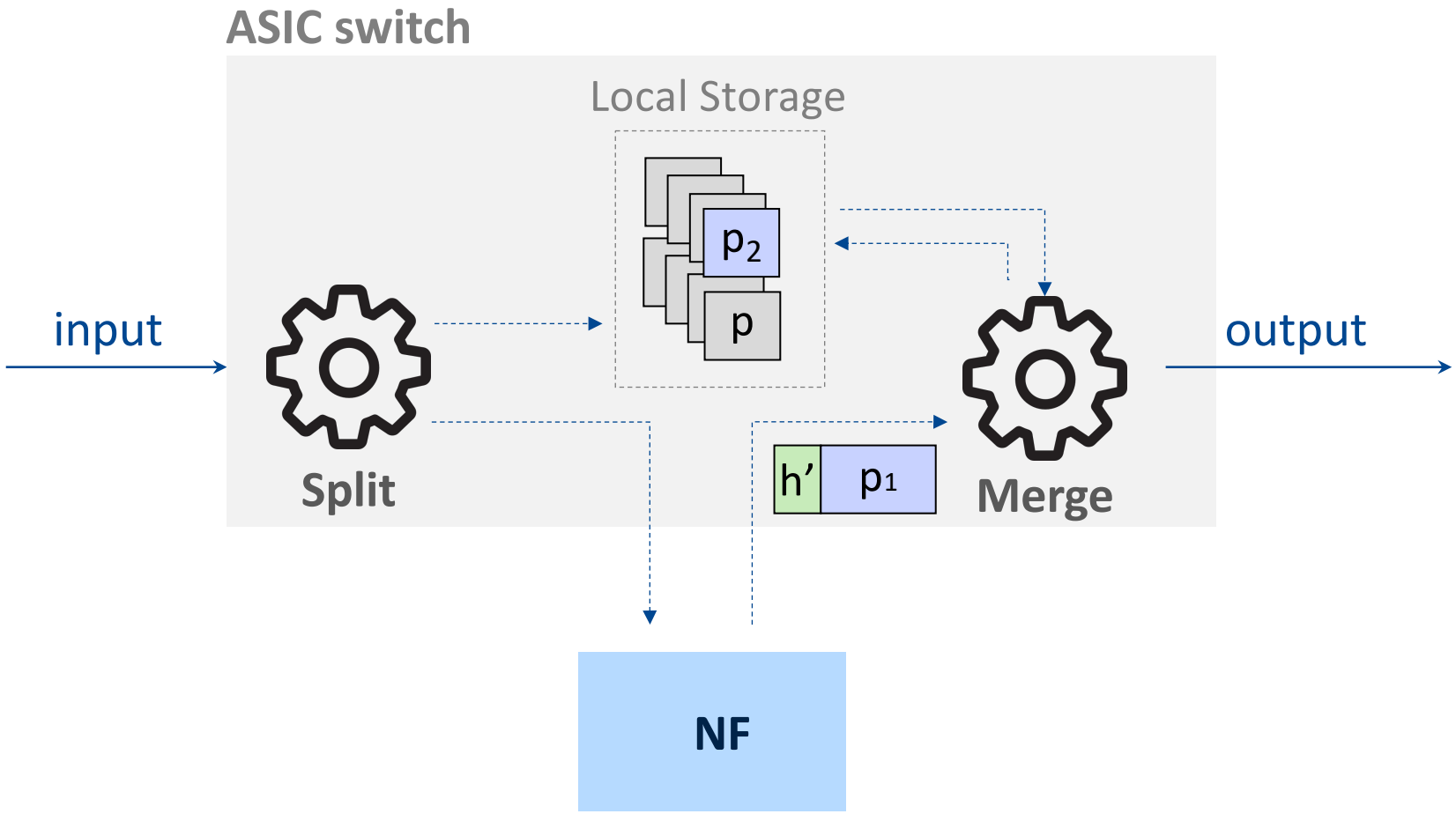

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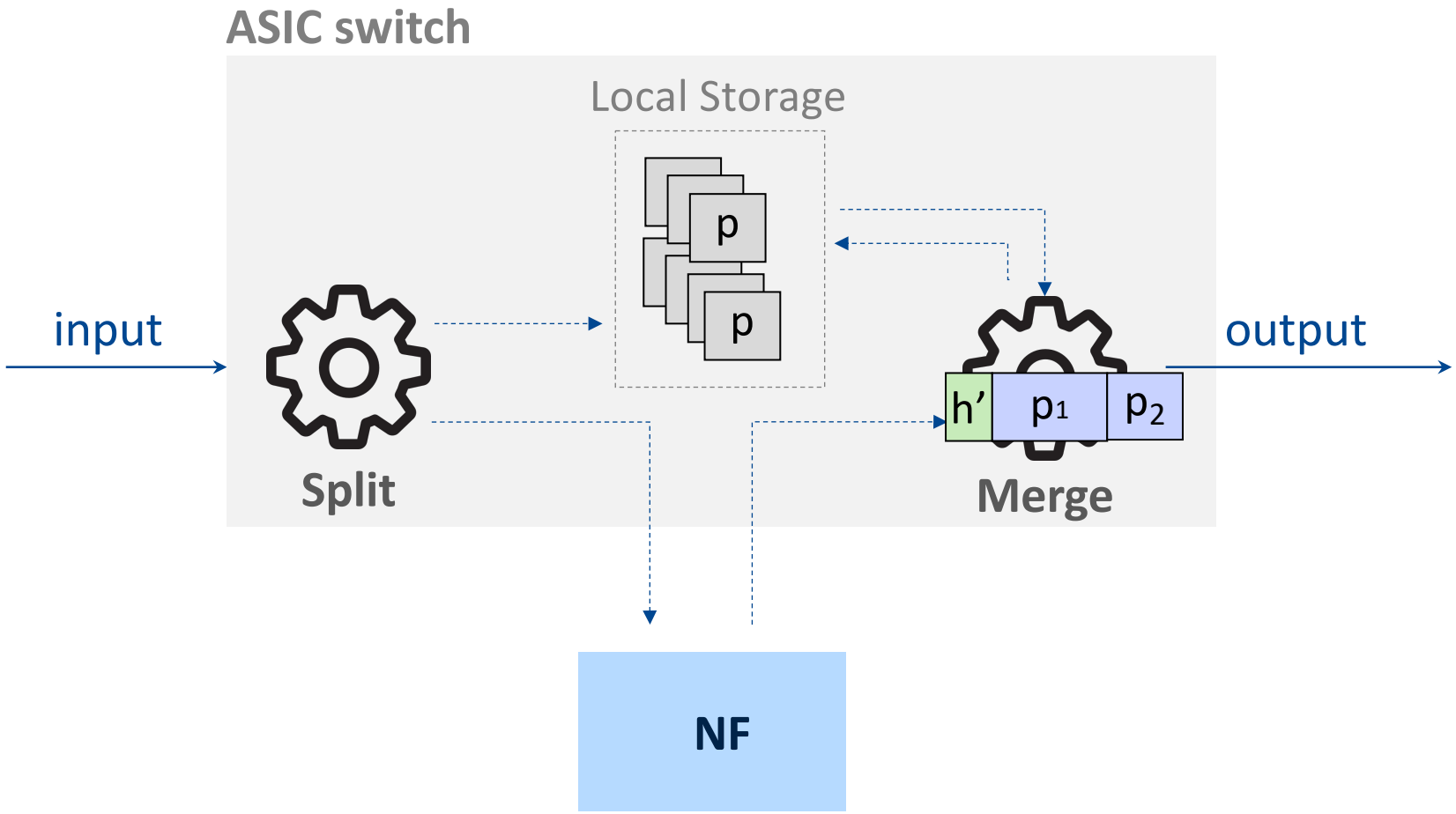
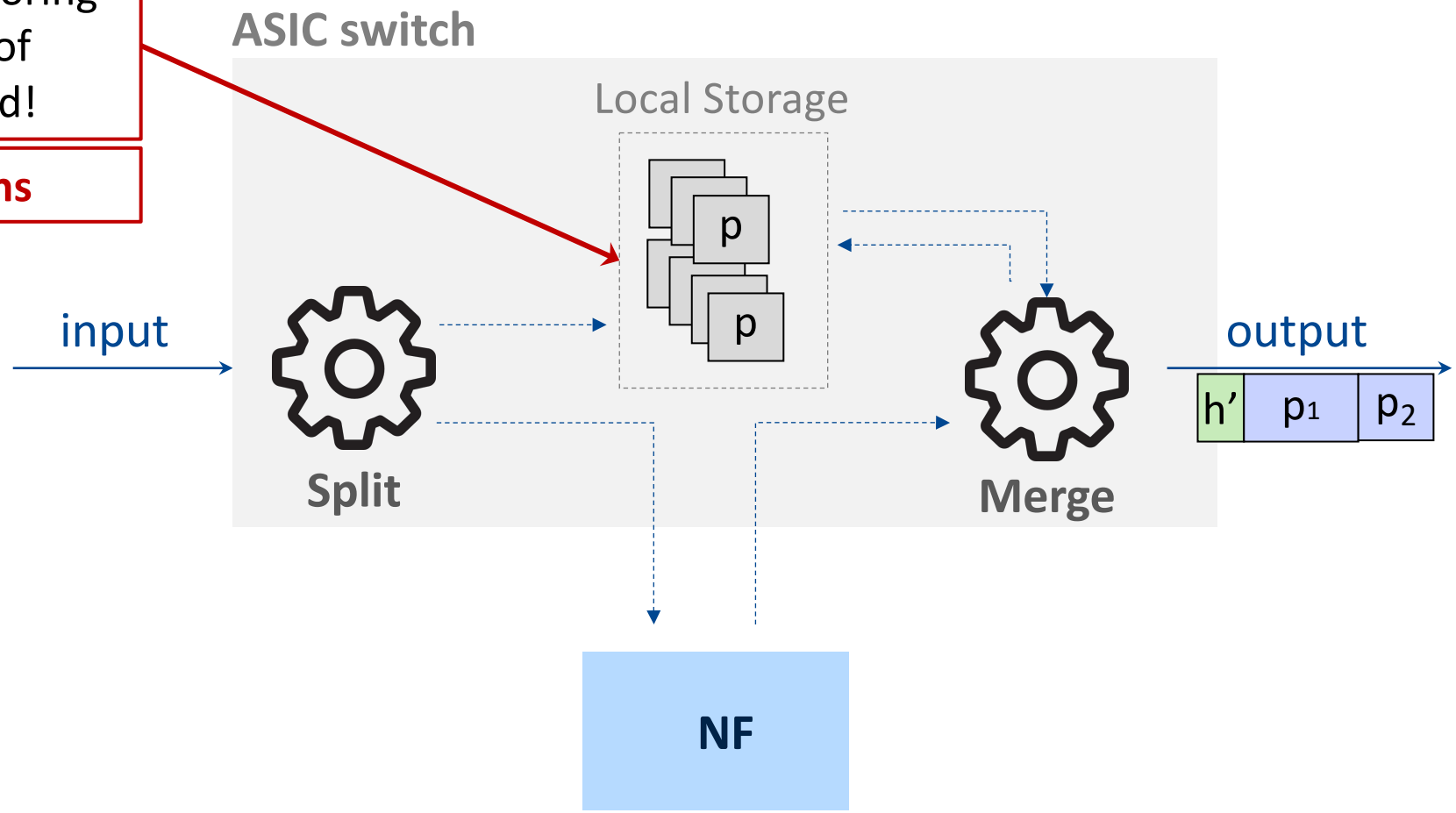


Storing a Few Bytes in ASIC SRAM (PayloadPark)

SRAM allows storing only a part of each payload!

Limited gains



Can we store the entire payload within the switch without requiring external devices?

Core Idea: A Queue-Based Packet Storage

Exploit the switch shared buffer to store payloads

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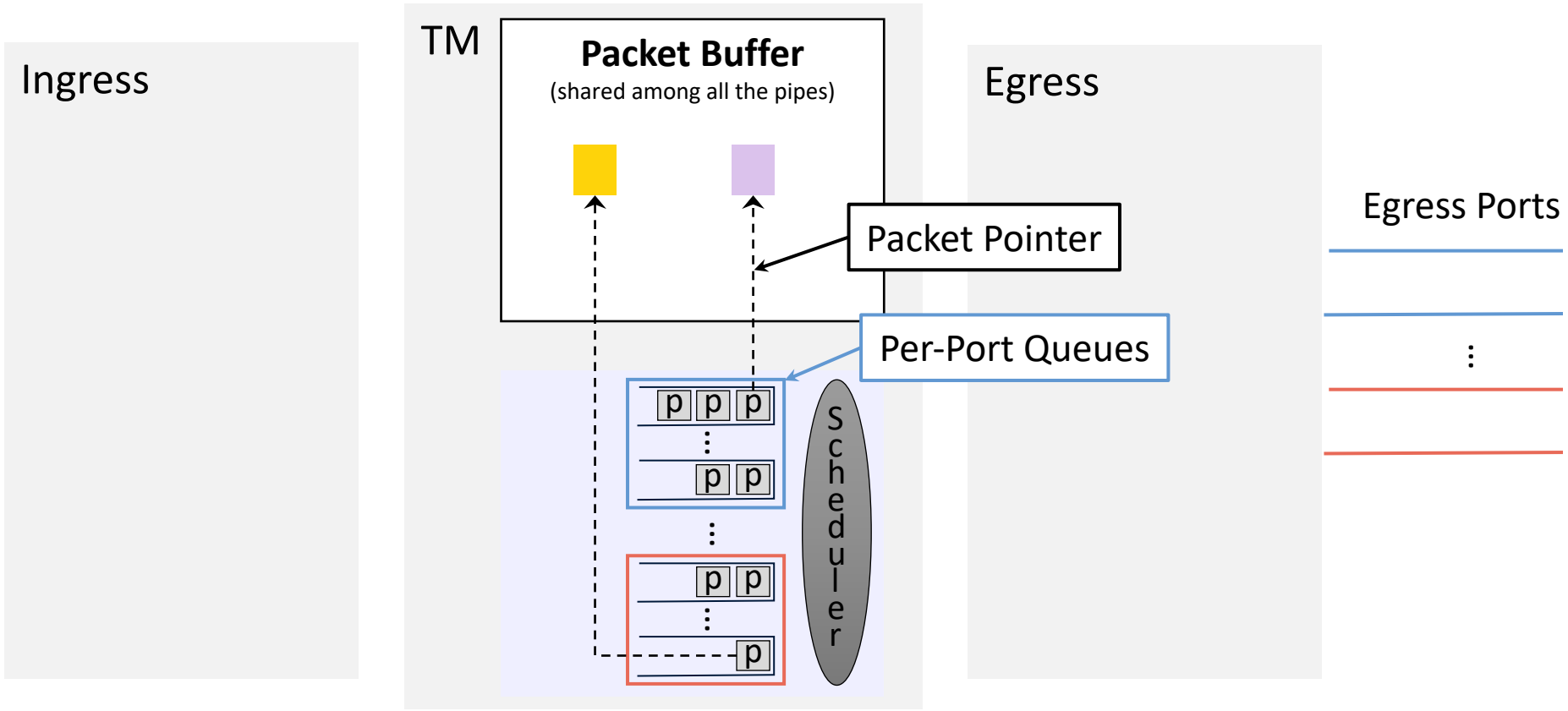

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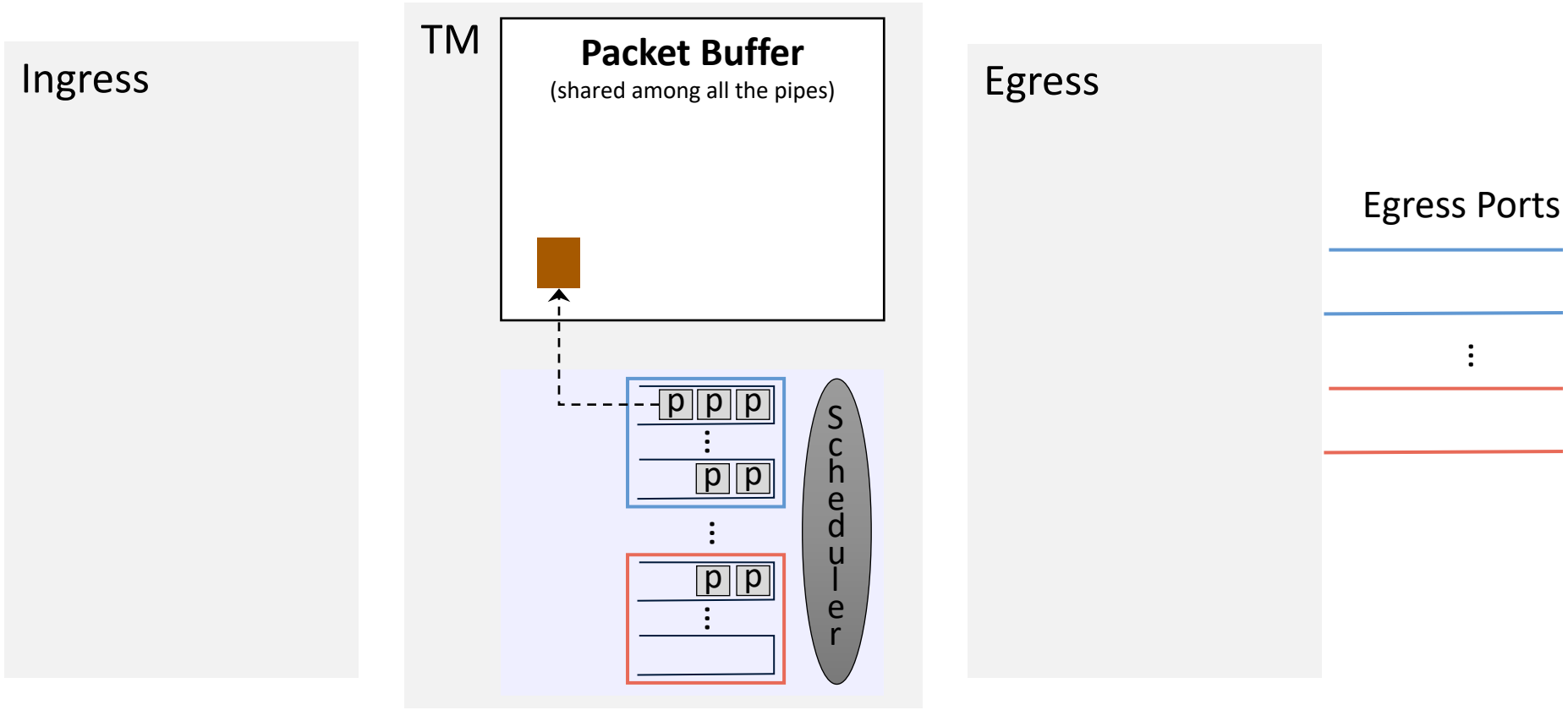


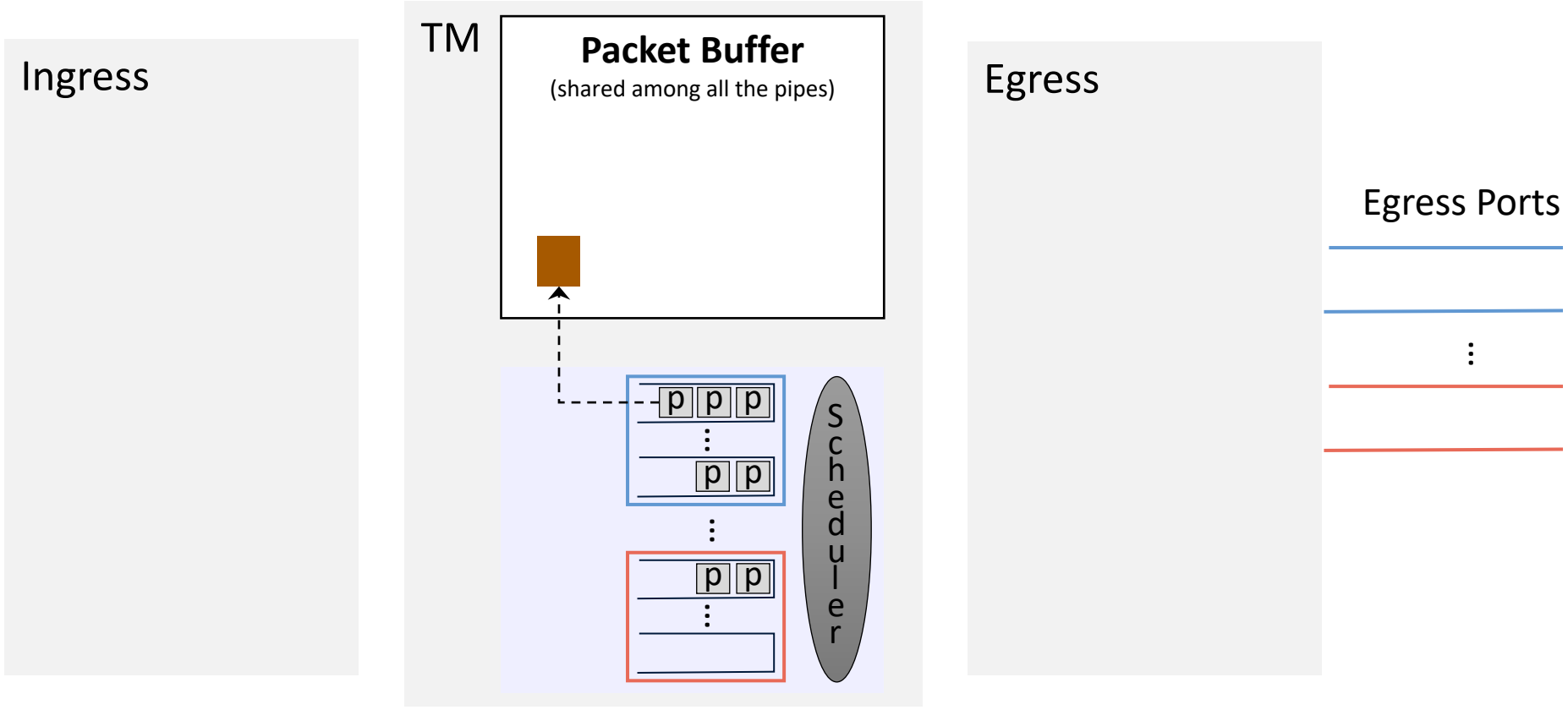
Core Idea: A Queue-Based Packet Storage

Exploit the switch shared buffer to store payloads

✓ Large shared buffer

✗ No programmatic access

? How can we access the packet buffer?



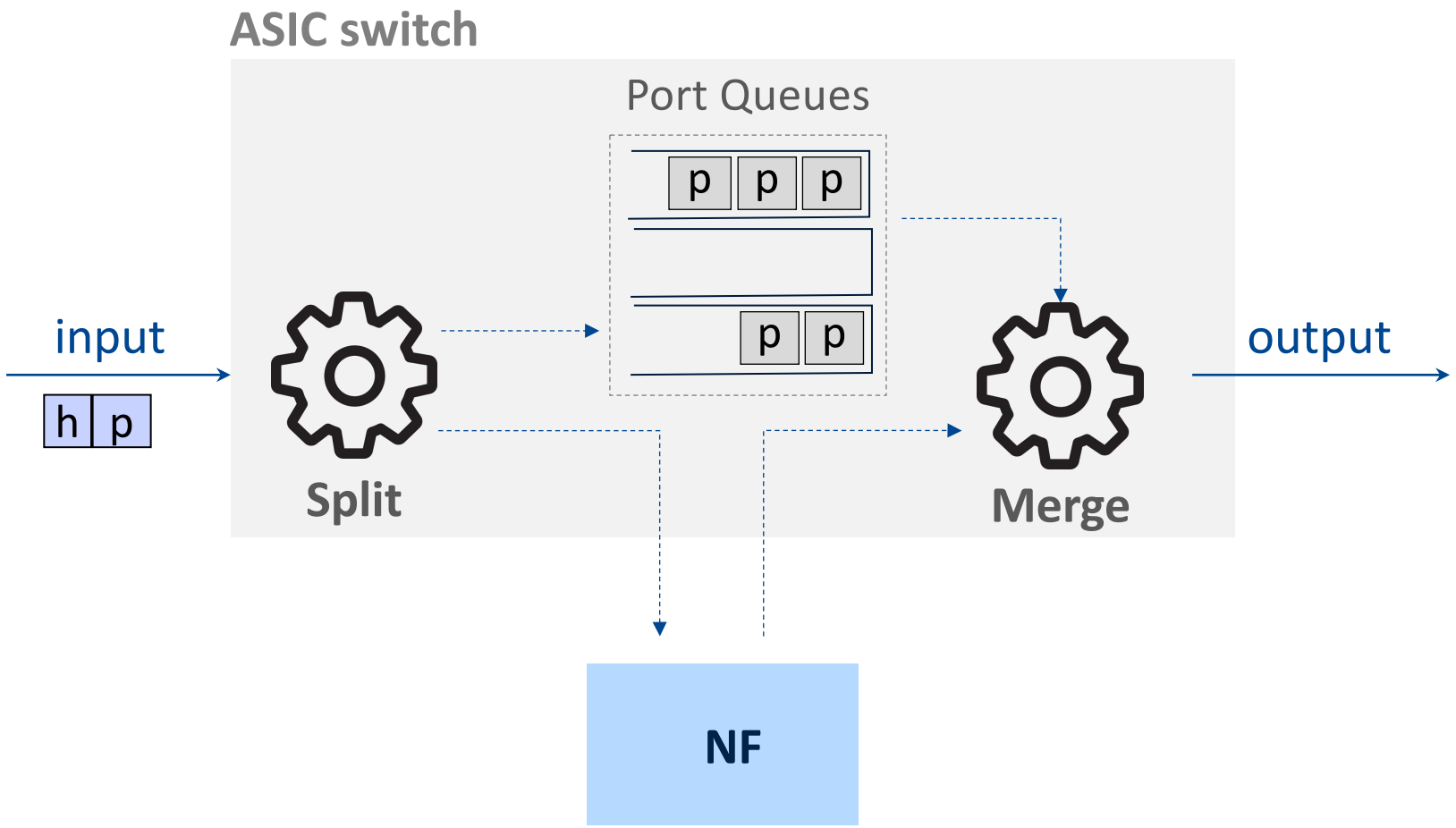
How can we access the packet buffer?

Enqueued packets **implicitly** control the buffer memory

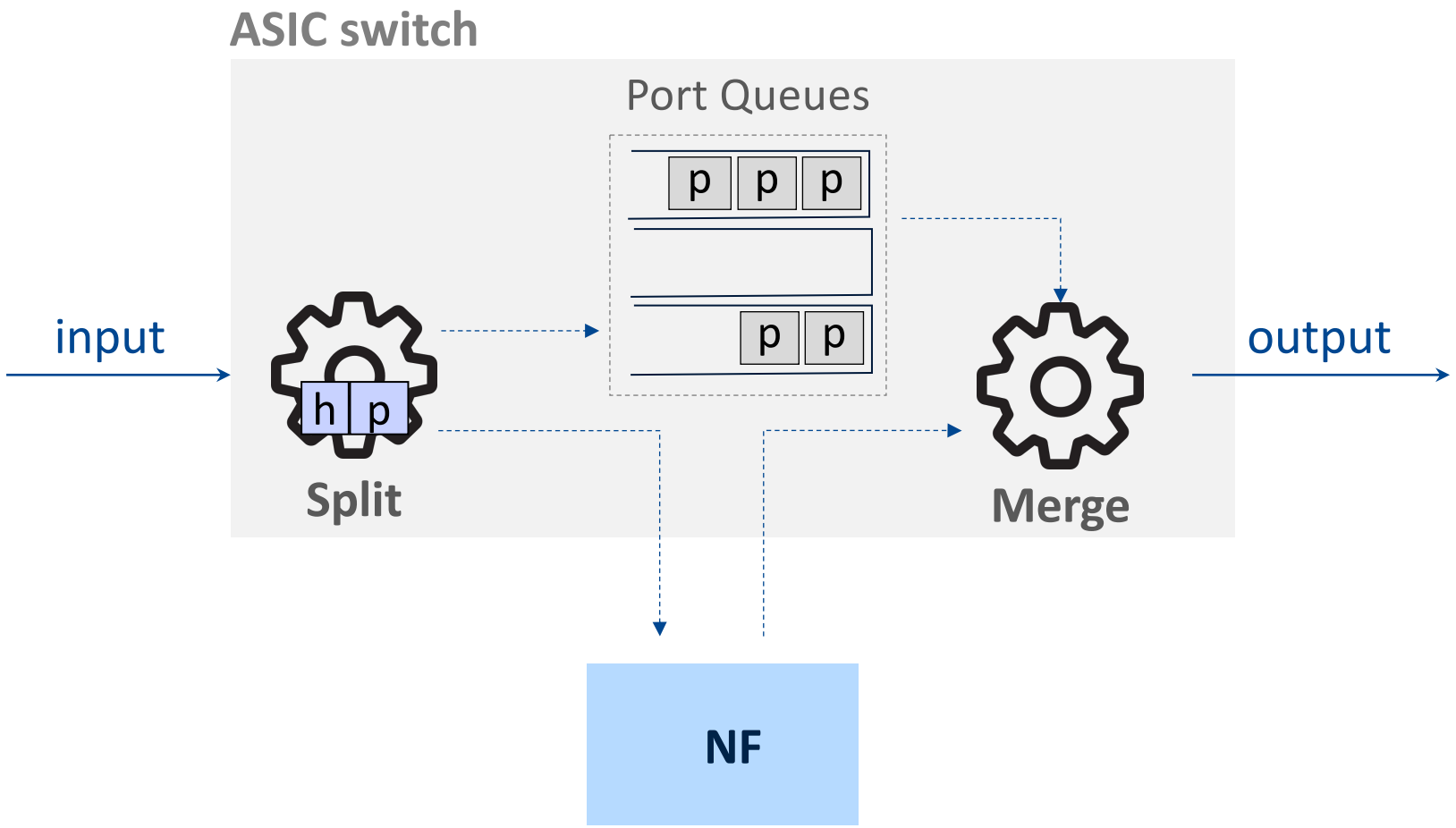
Hold payloads in the port queues until
the processed header from the NF is returned!

Would it work for real?

Challenges


ASIC switch
Port Queues
p
p
p
p
p
input
h
p
Split
Merge
output
NF

Challenges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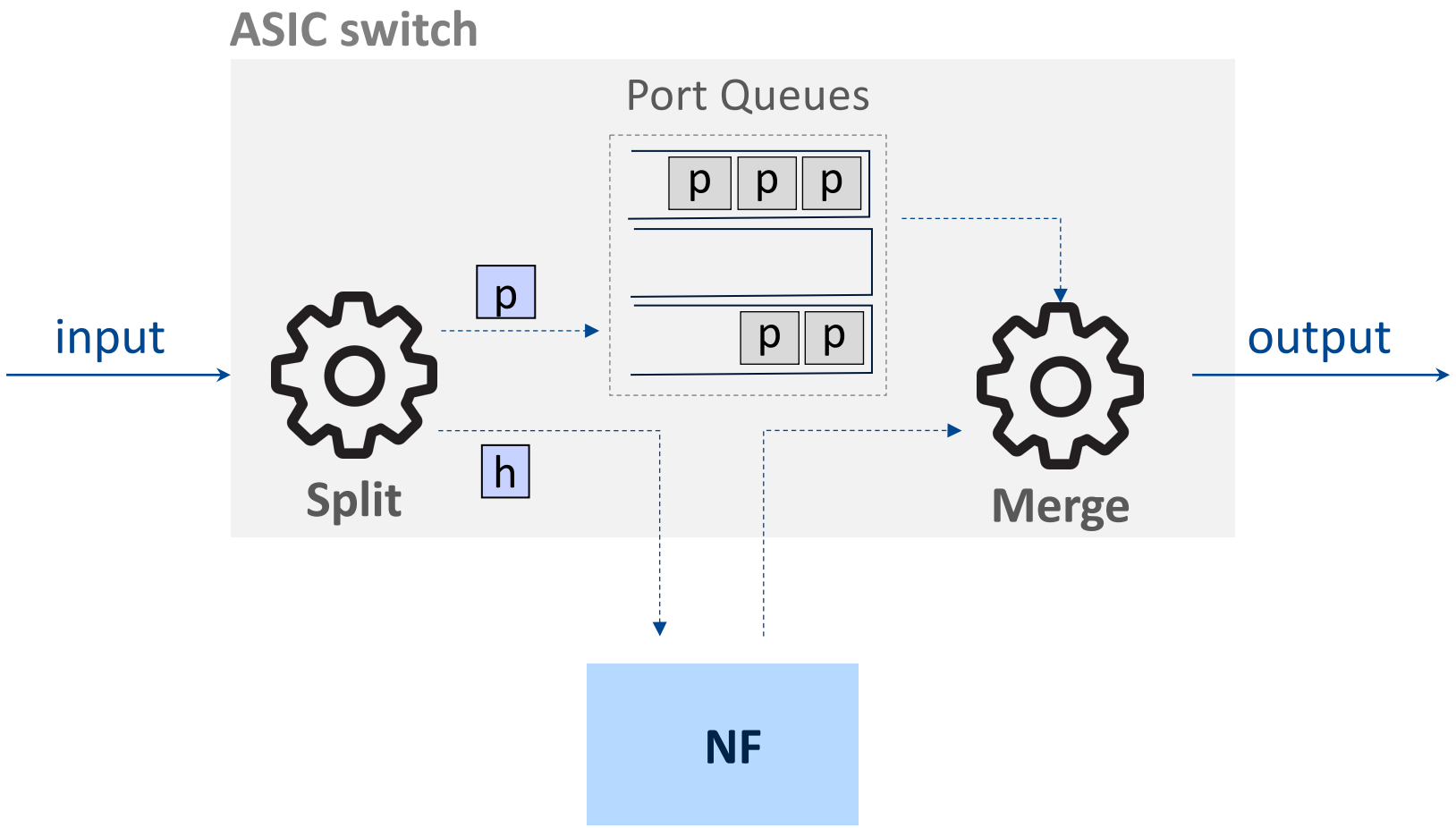
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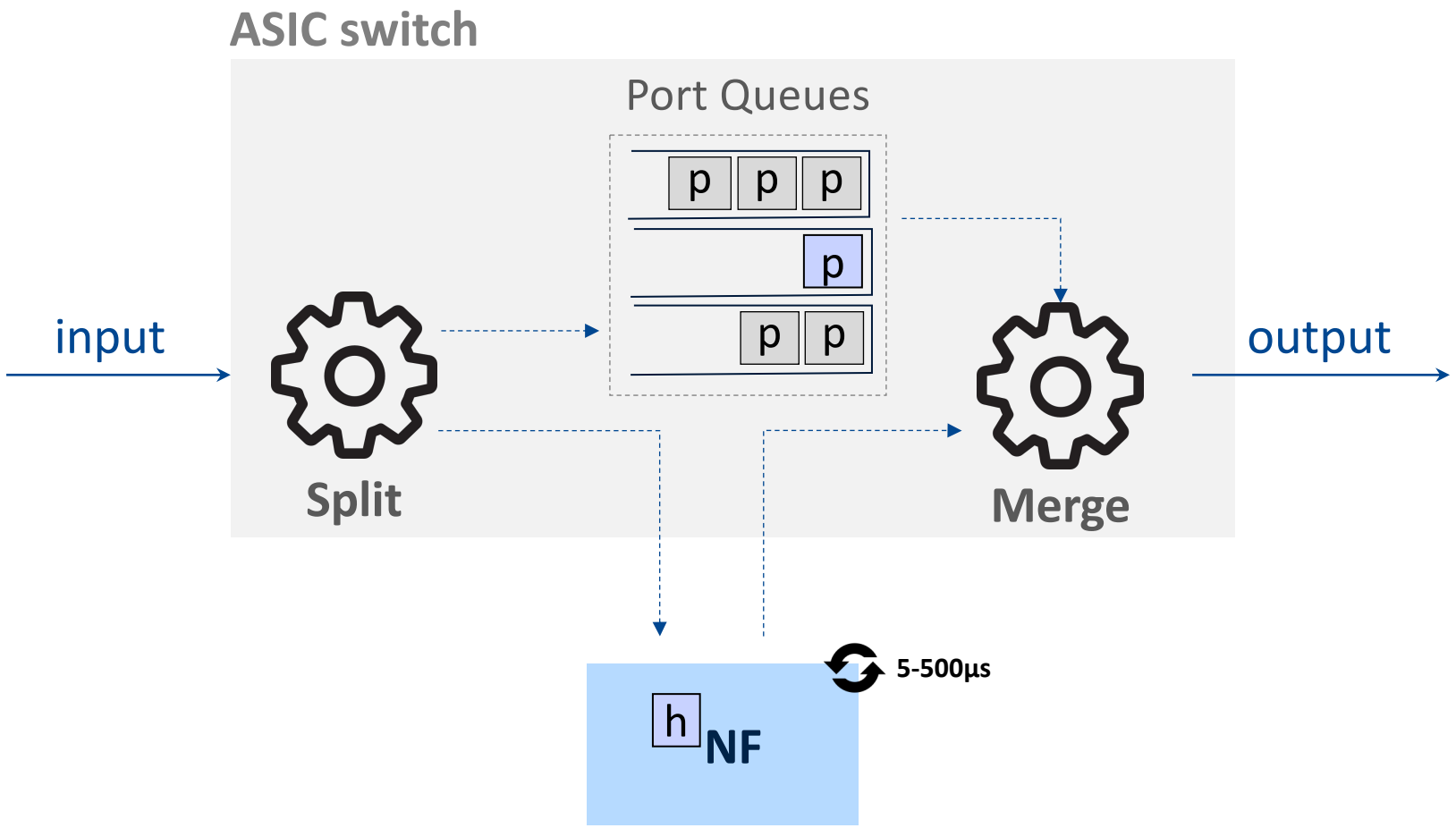
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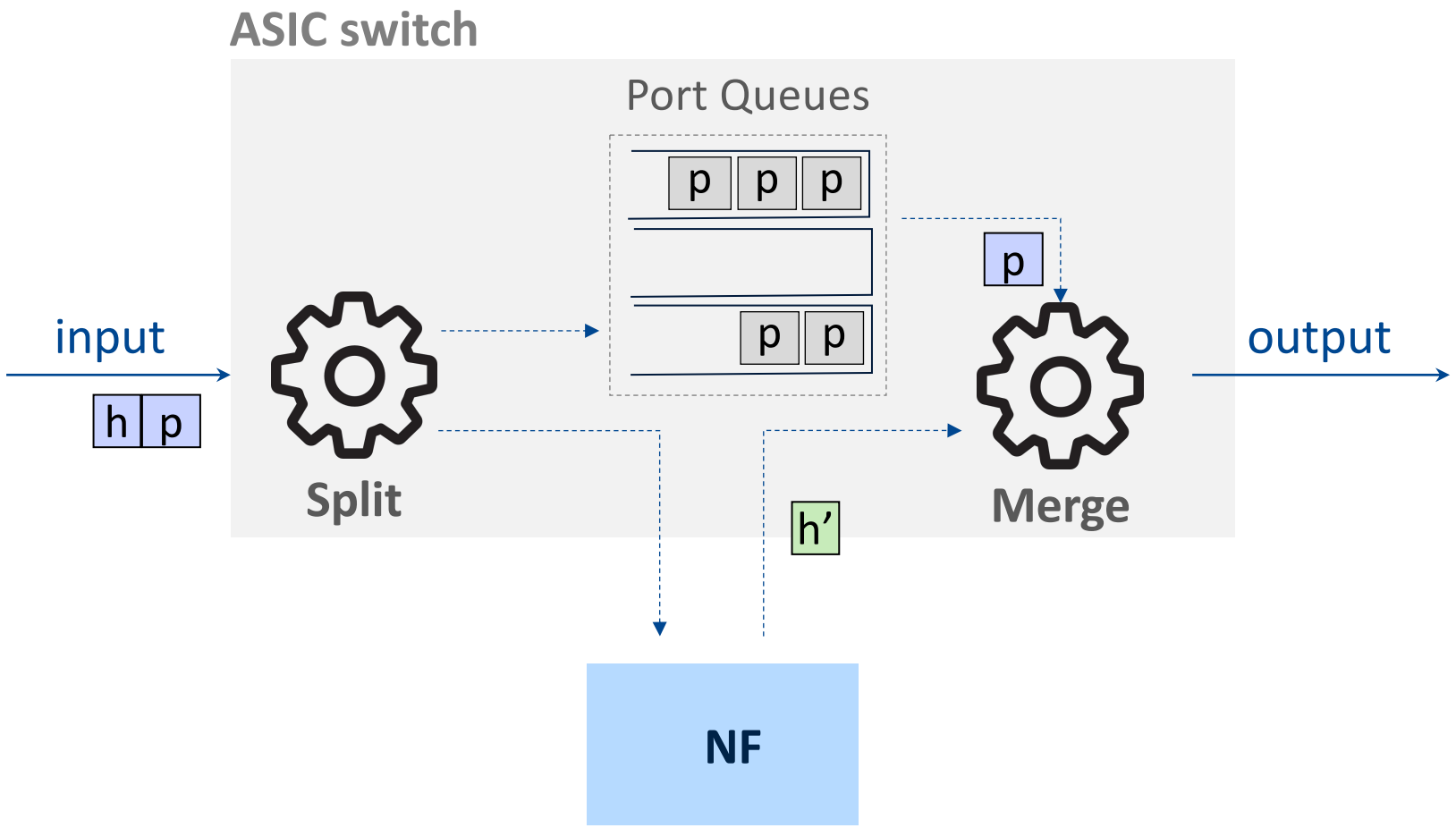
5-500µs

Challenges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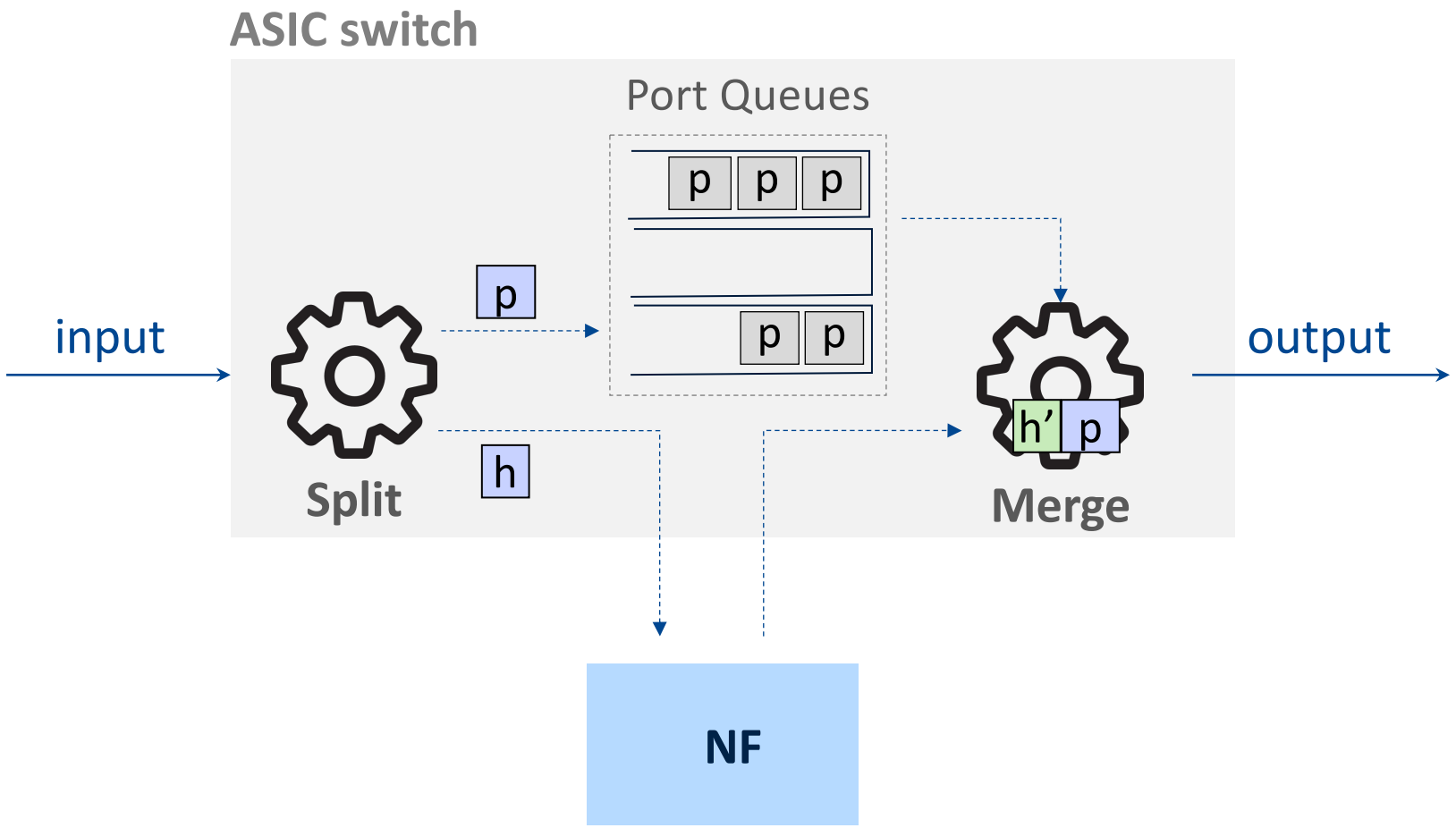
Challenges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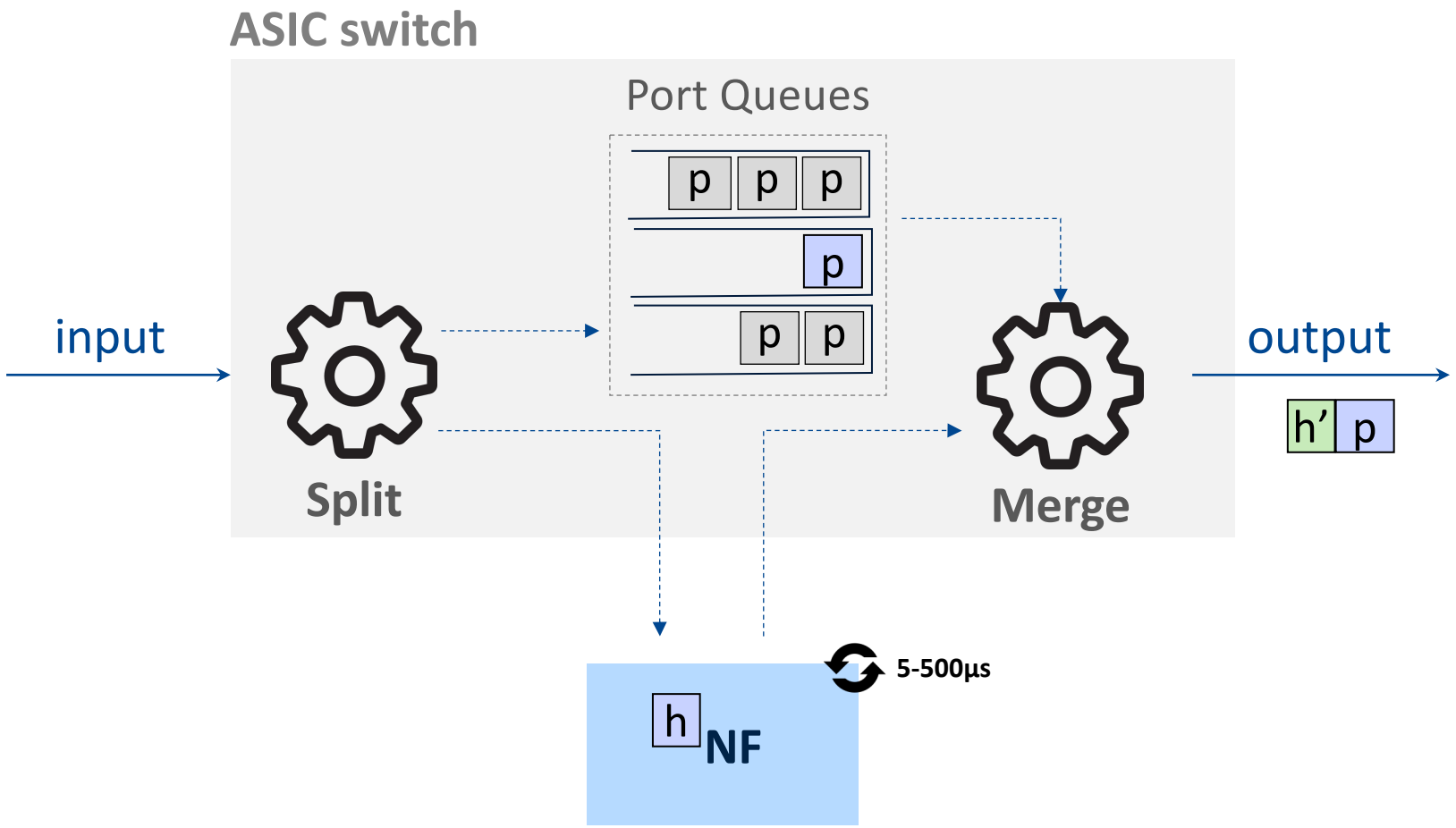
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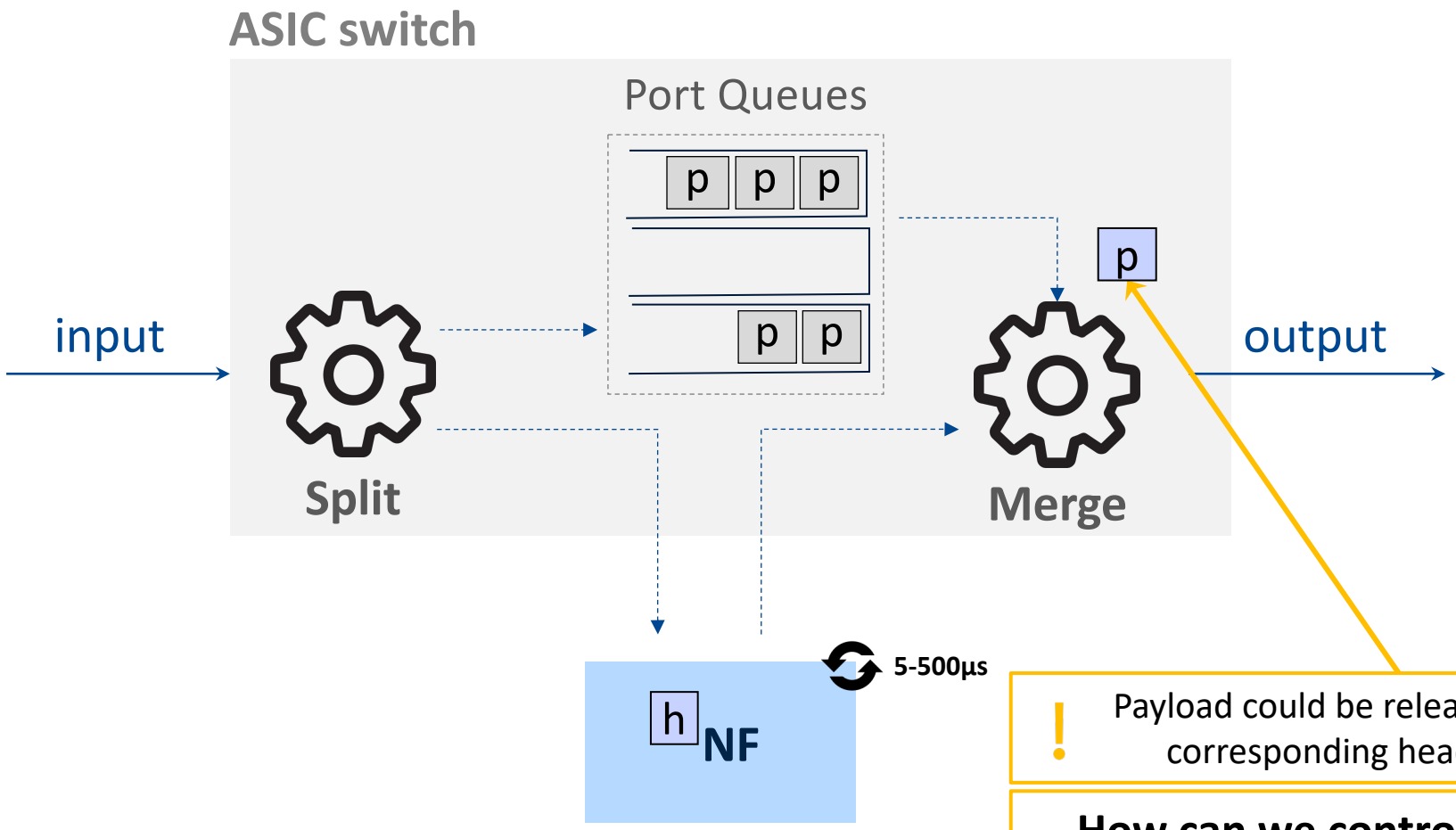
ASIC switch
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Payload could be released before the corresponding header is back!
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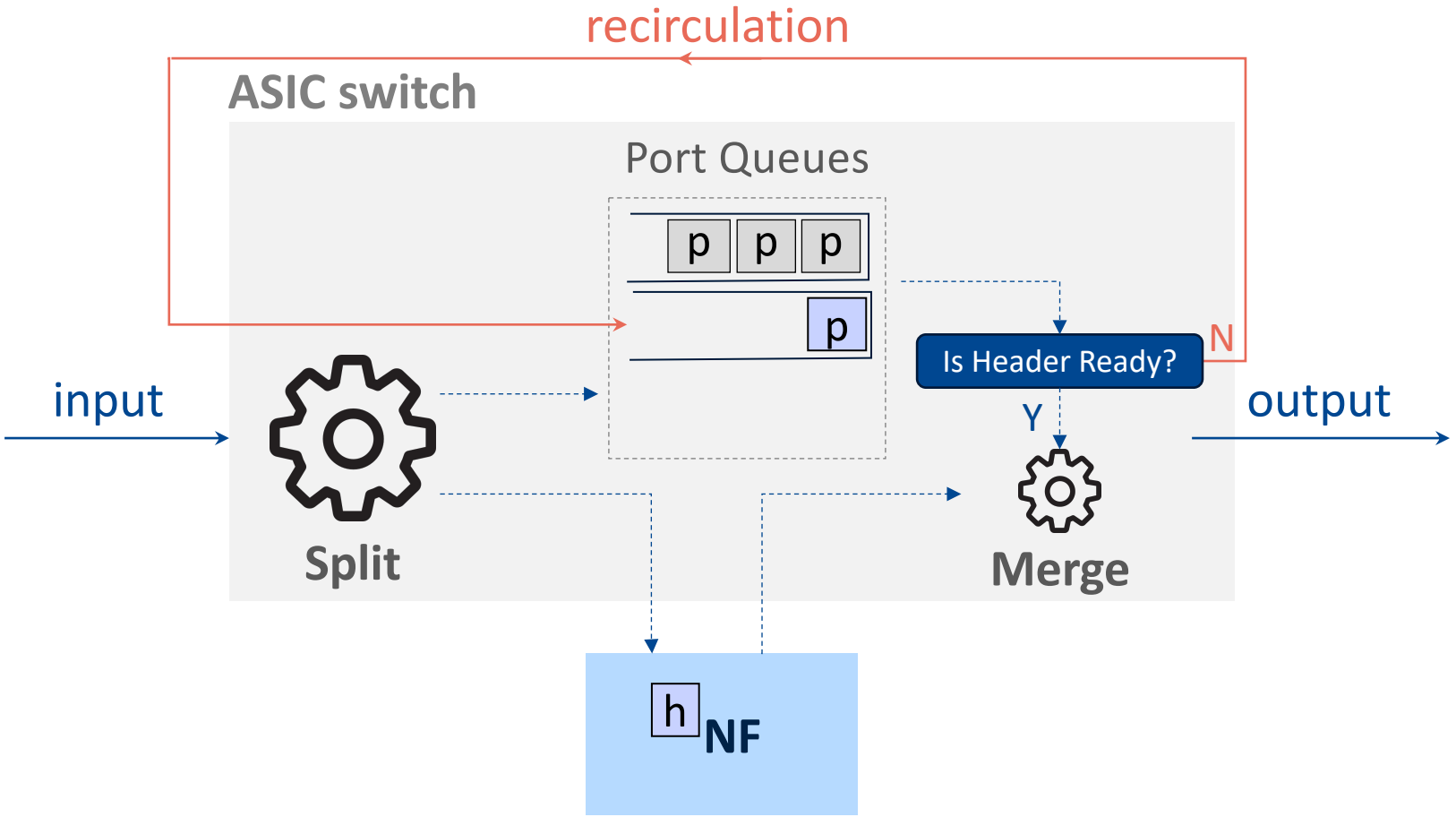

TurboSwitch

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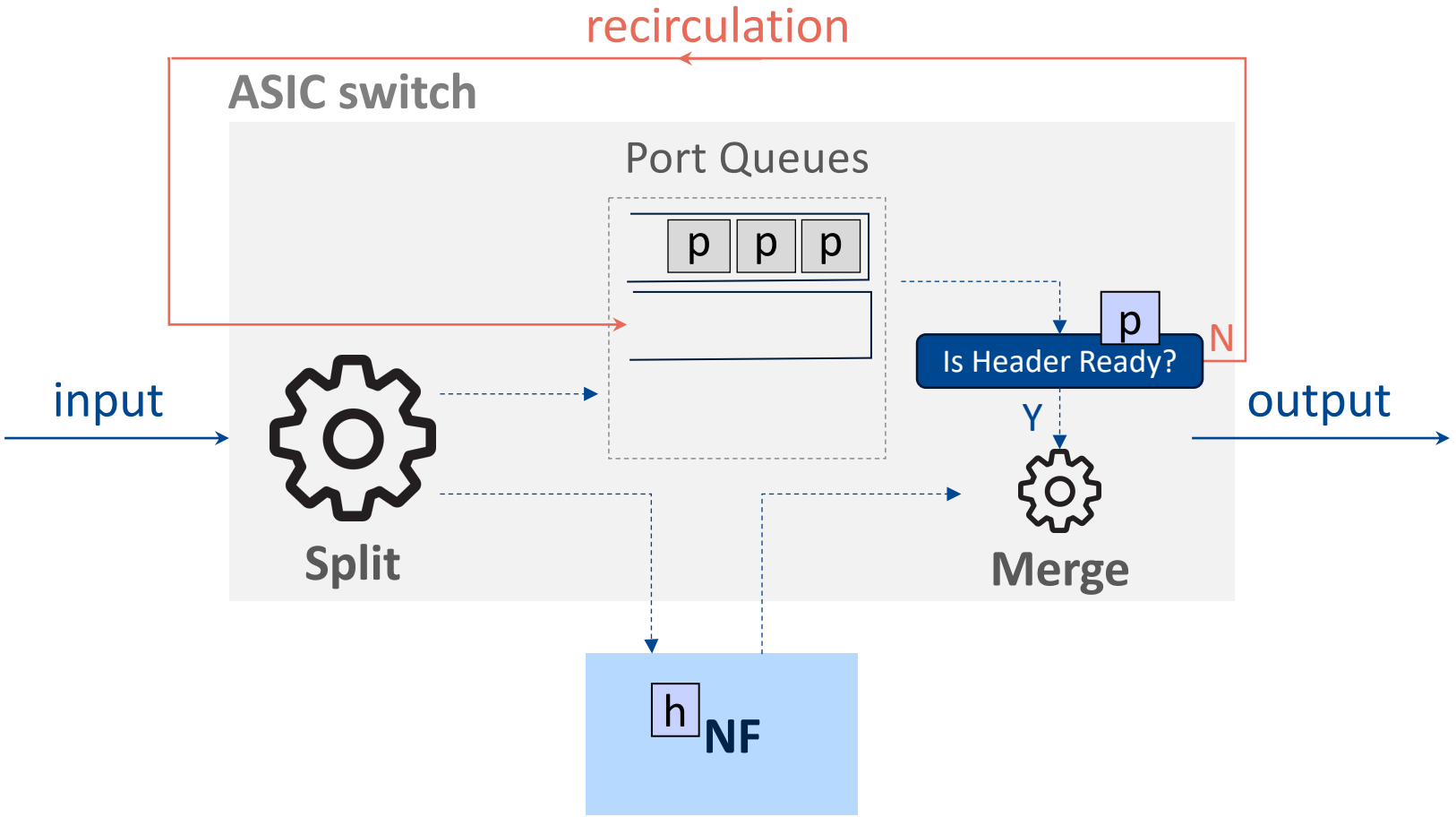

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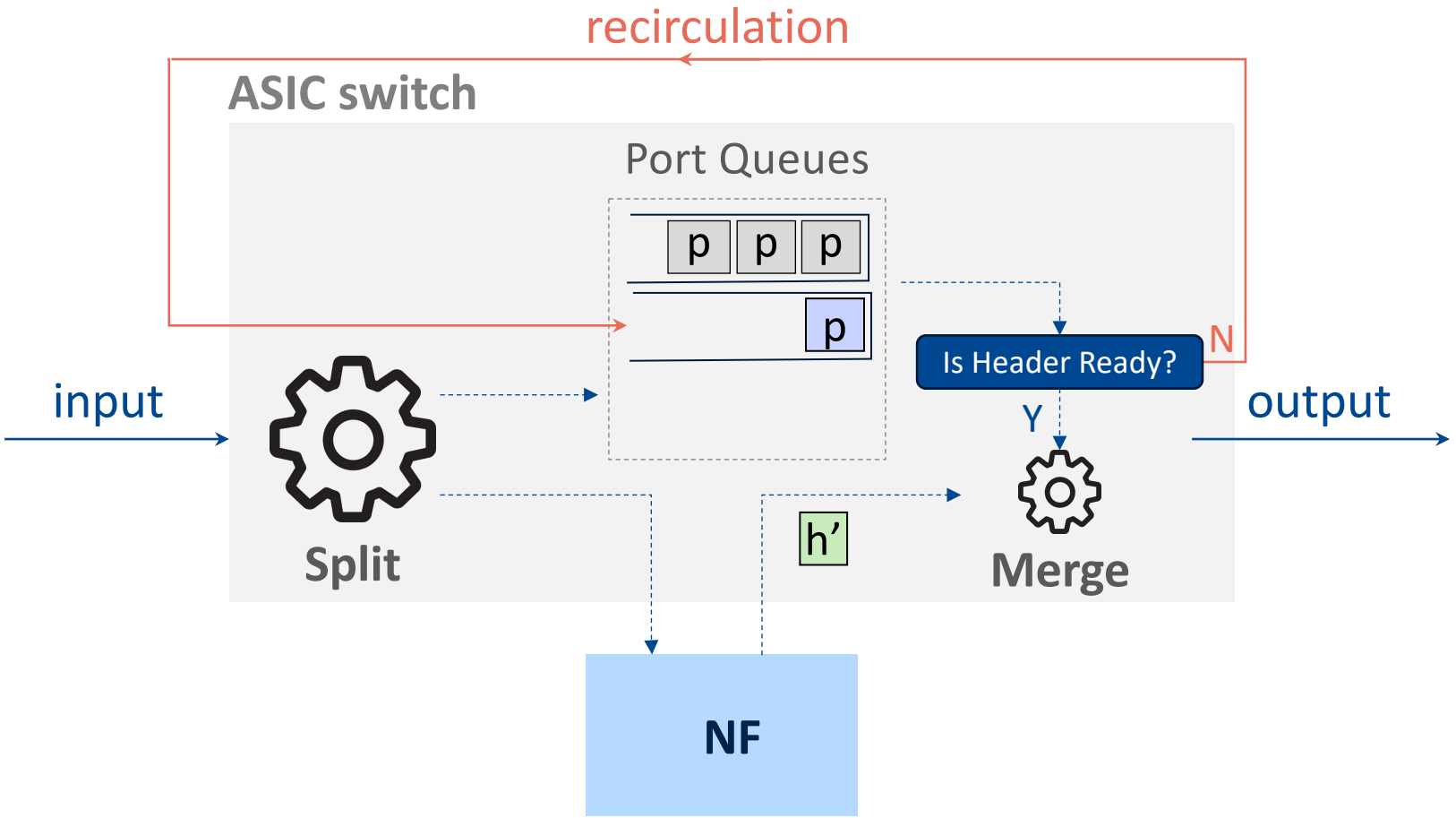

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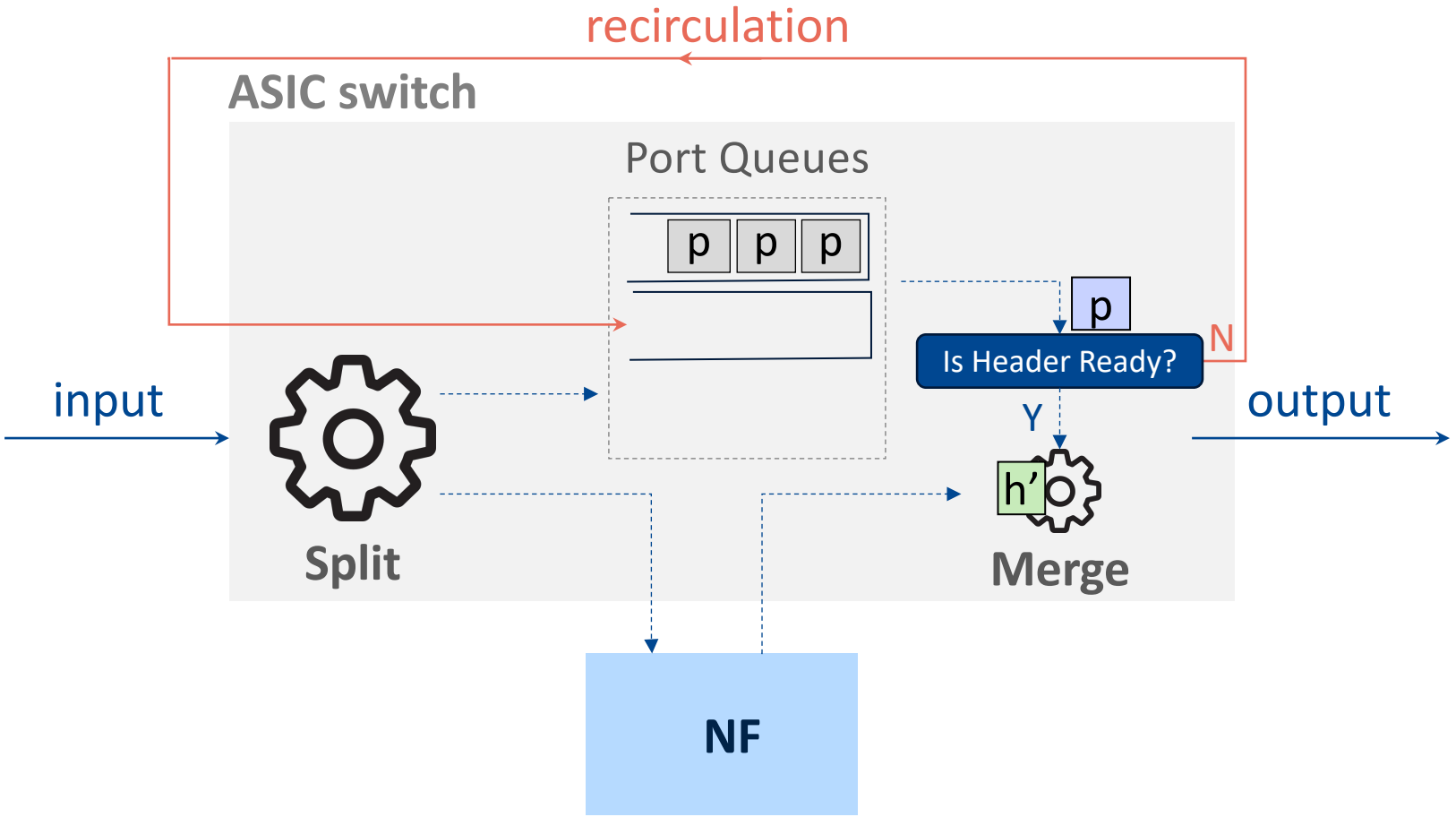

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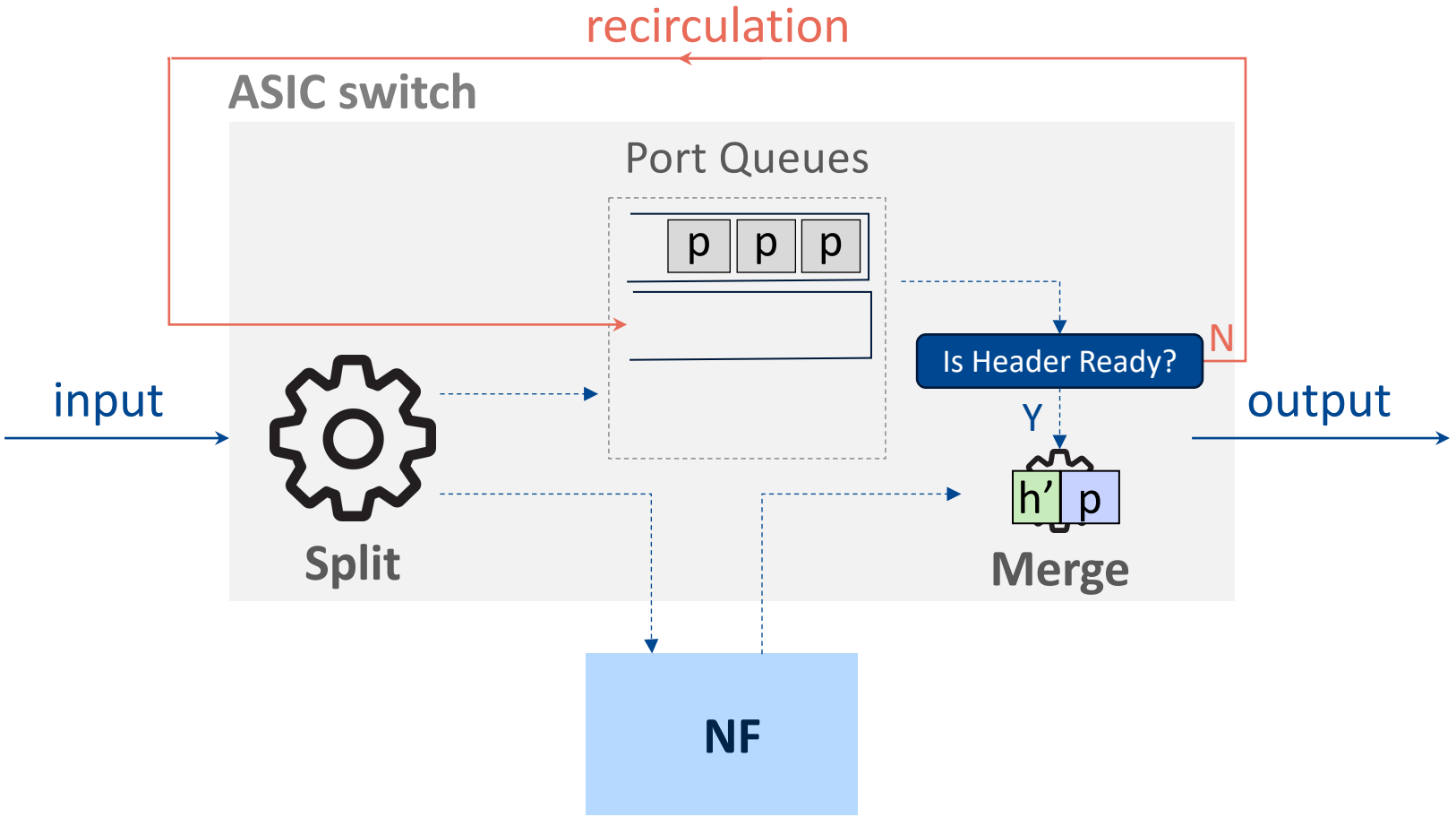

TurboSwitch

Recirculate payloads until headers are ready

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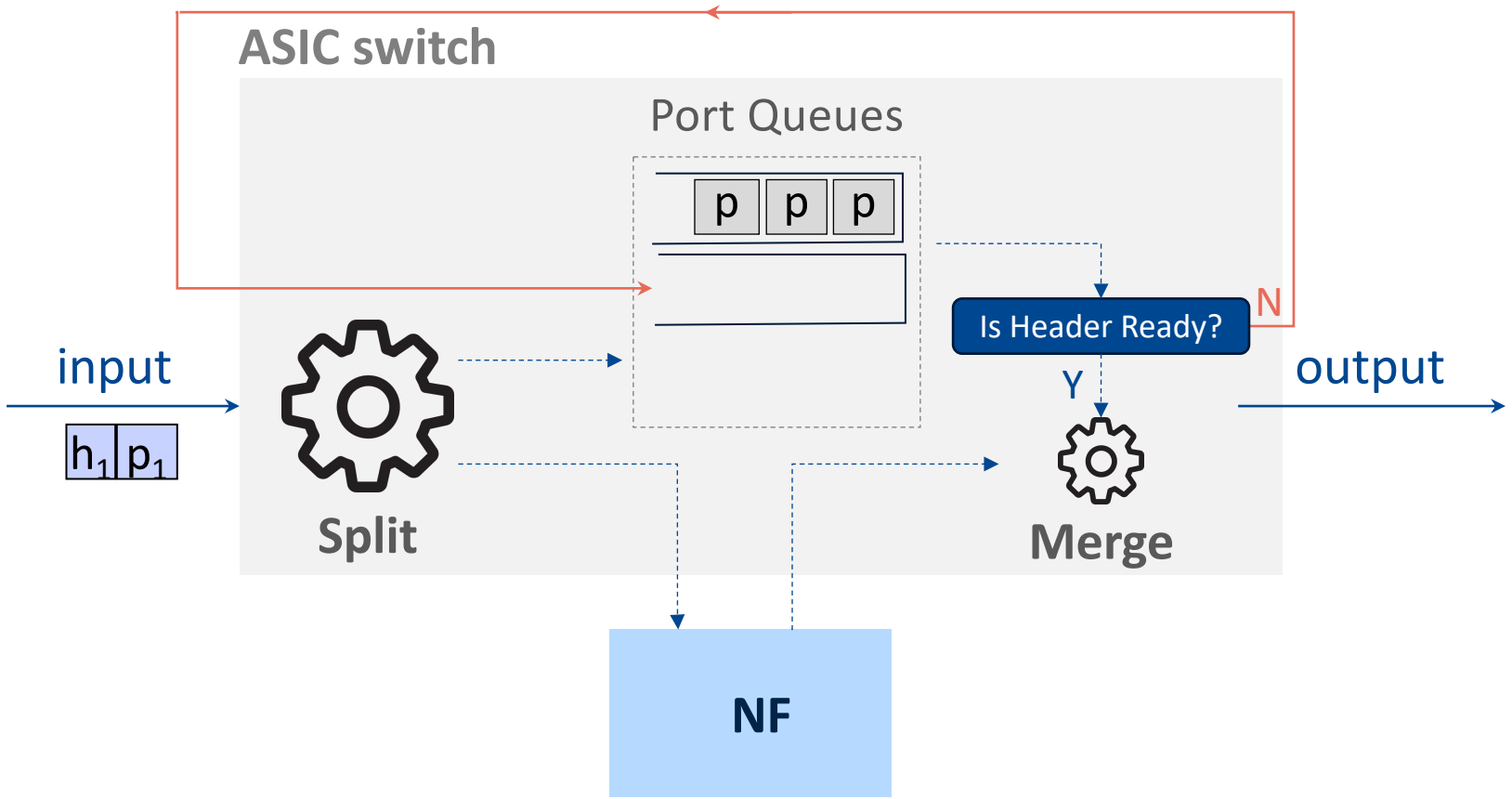
Queue **self-clocking**



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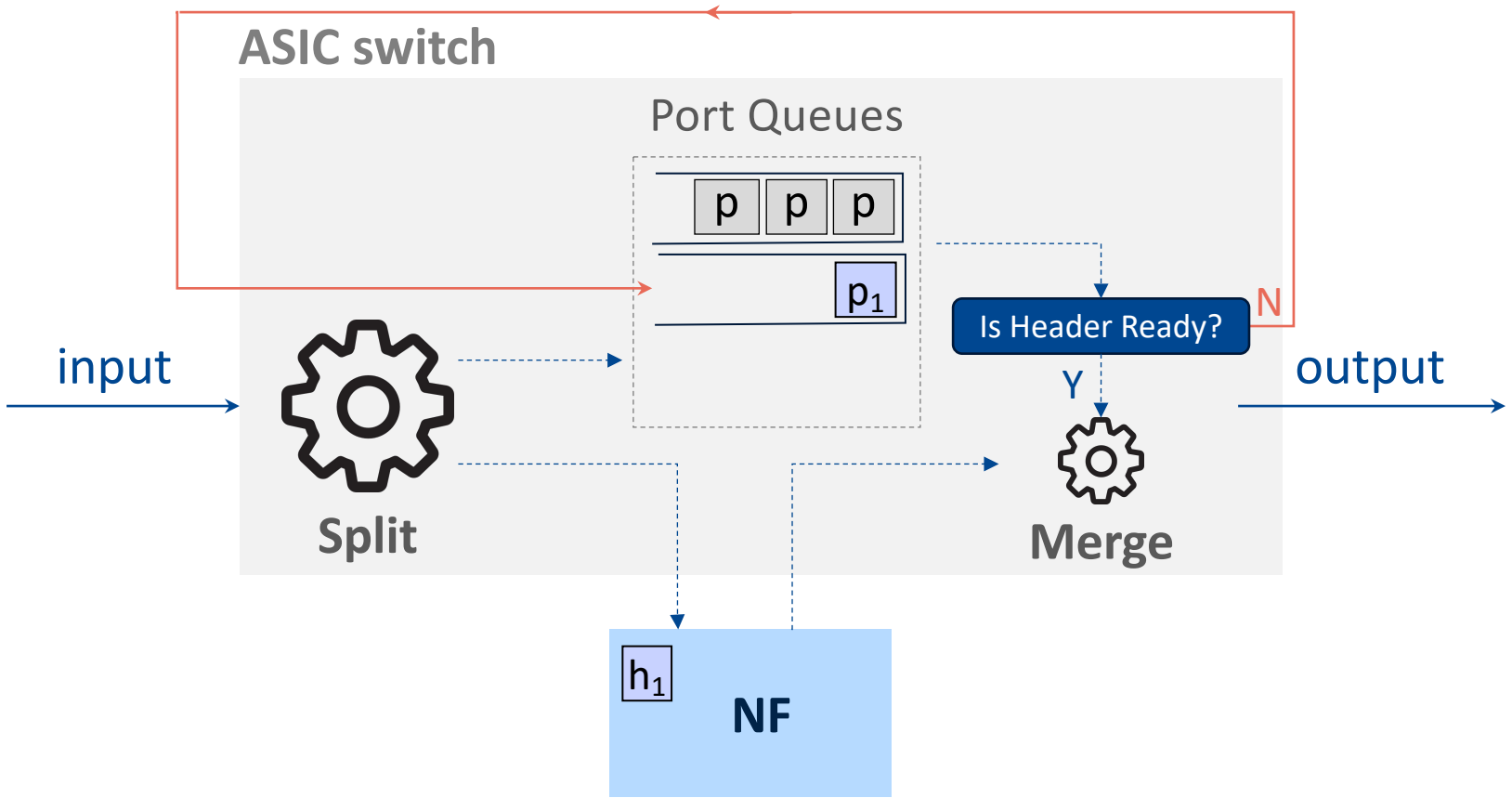

TurboSwitch

Recirculate payloads until headers are ready

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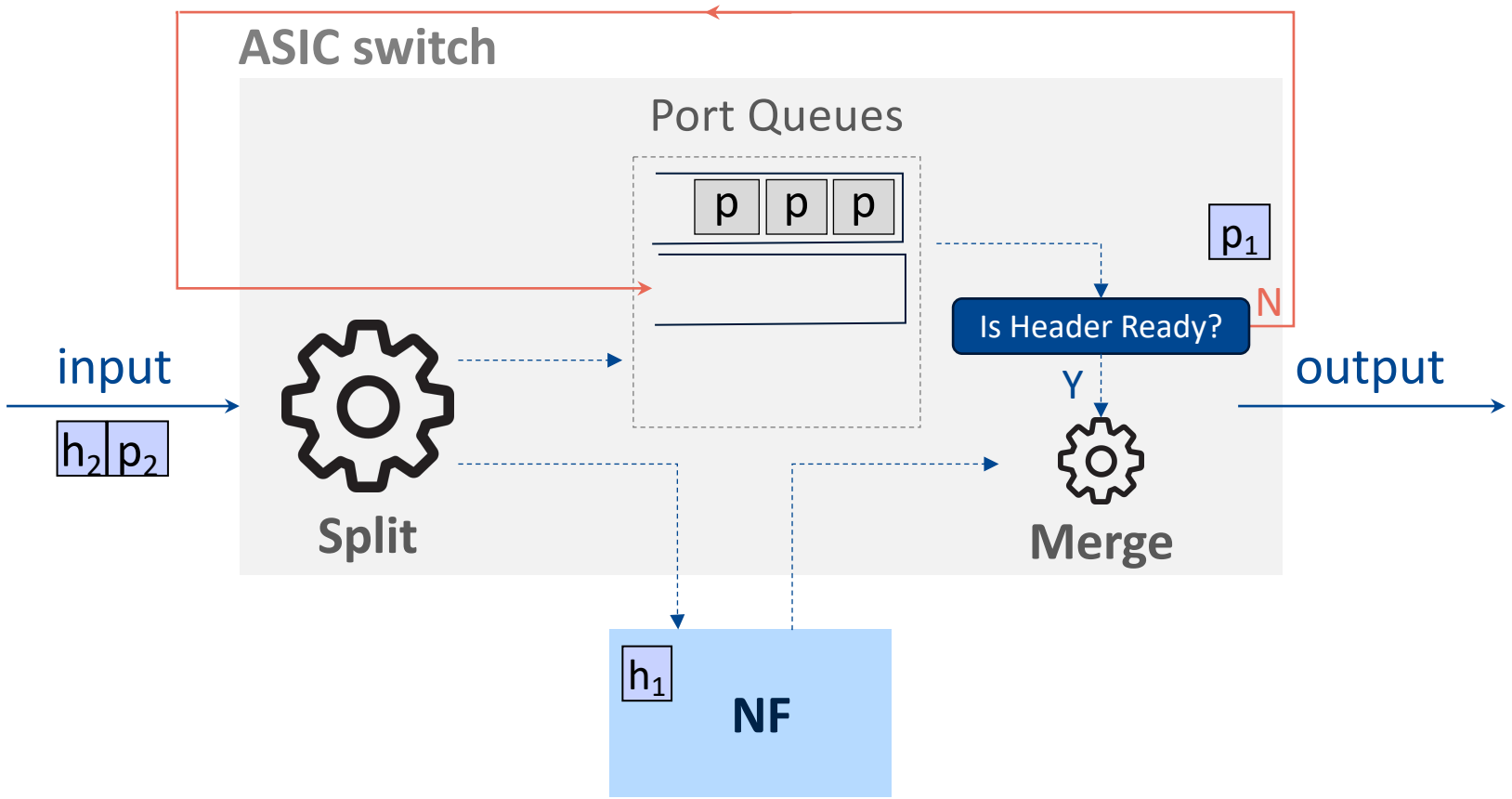

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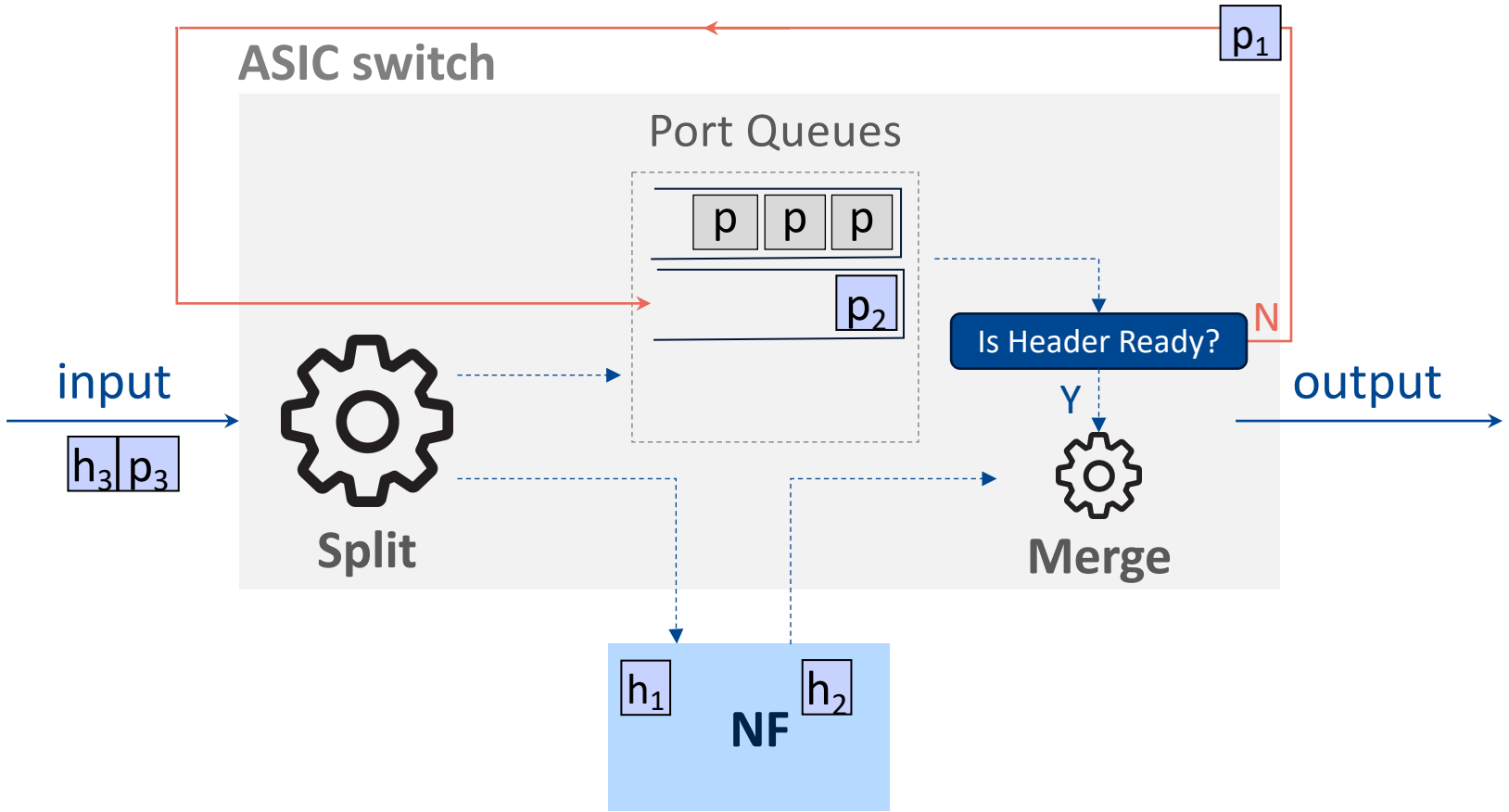

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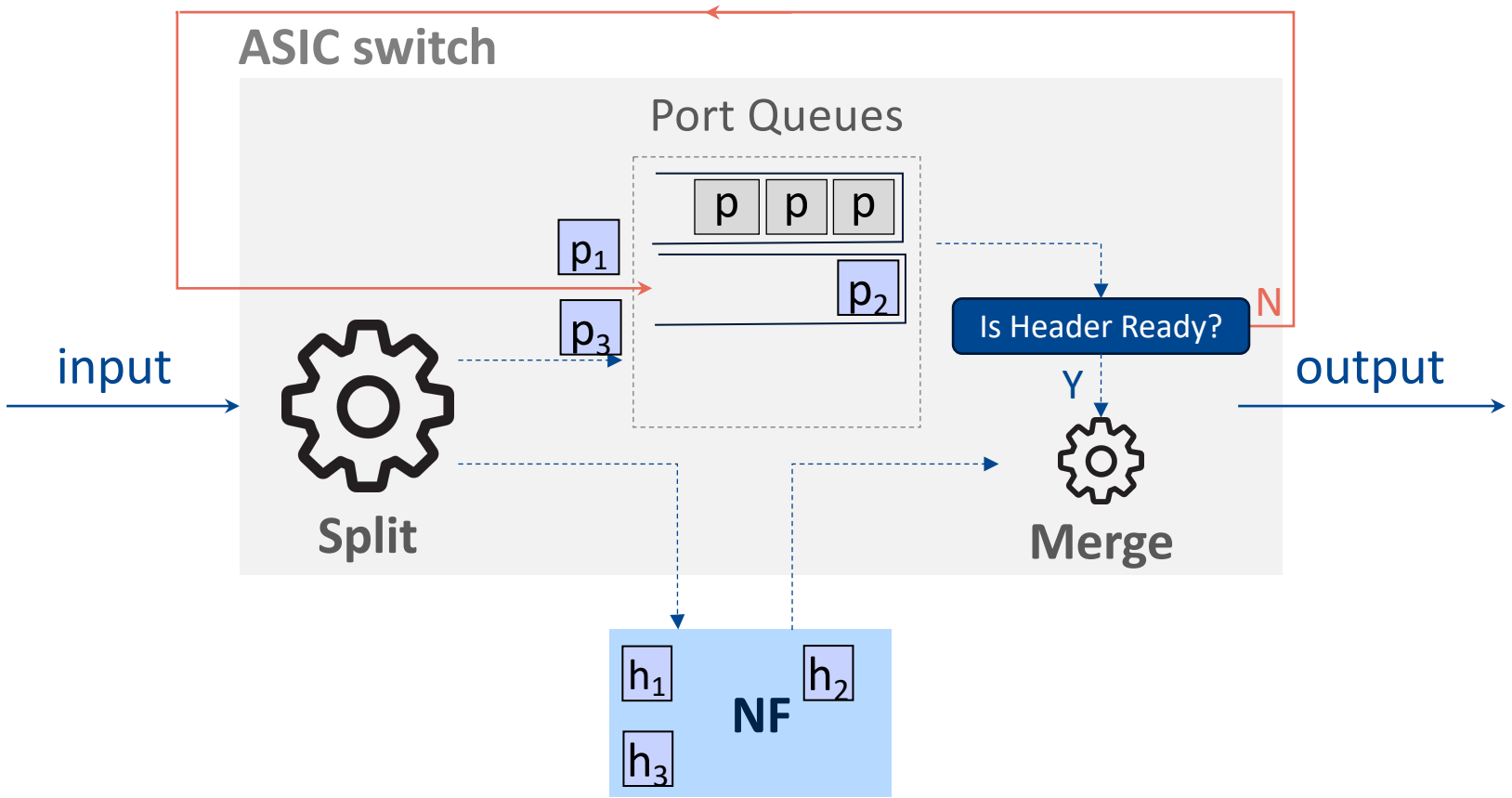

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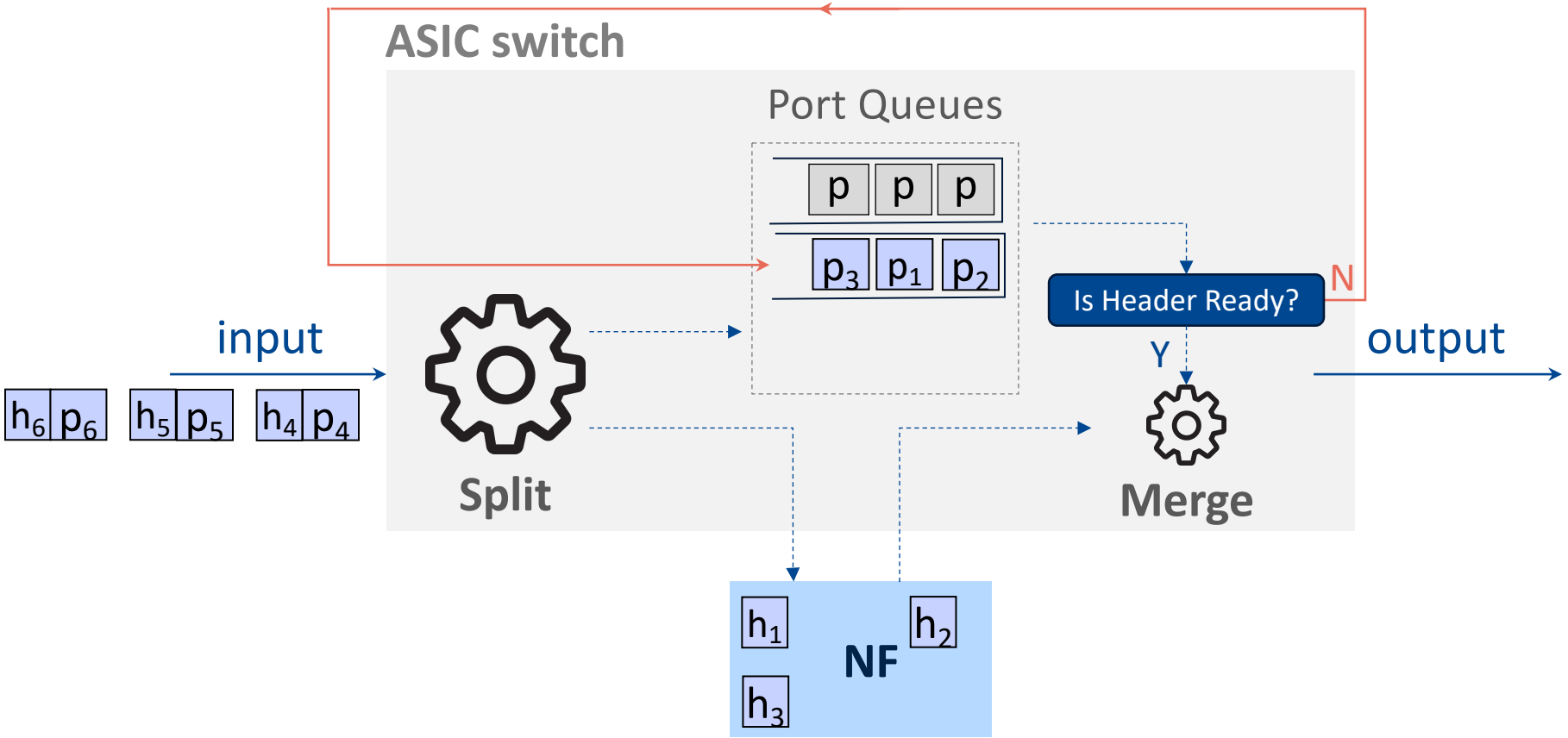

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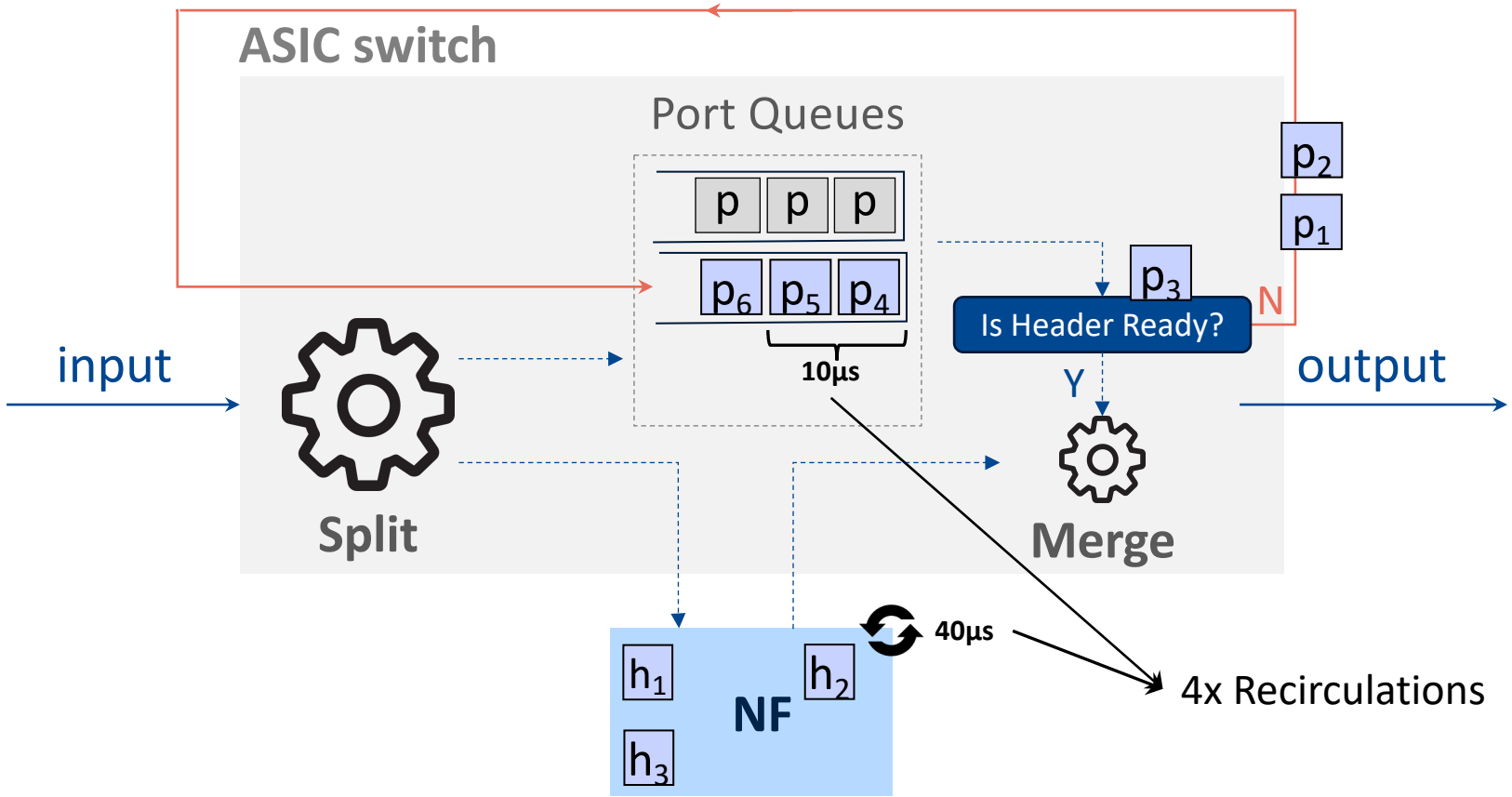


TurboSwitch

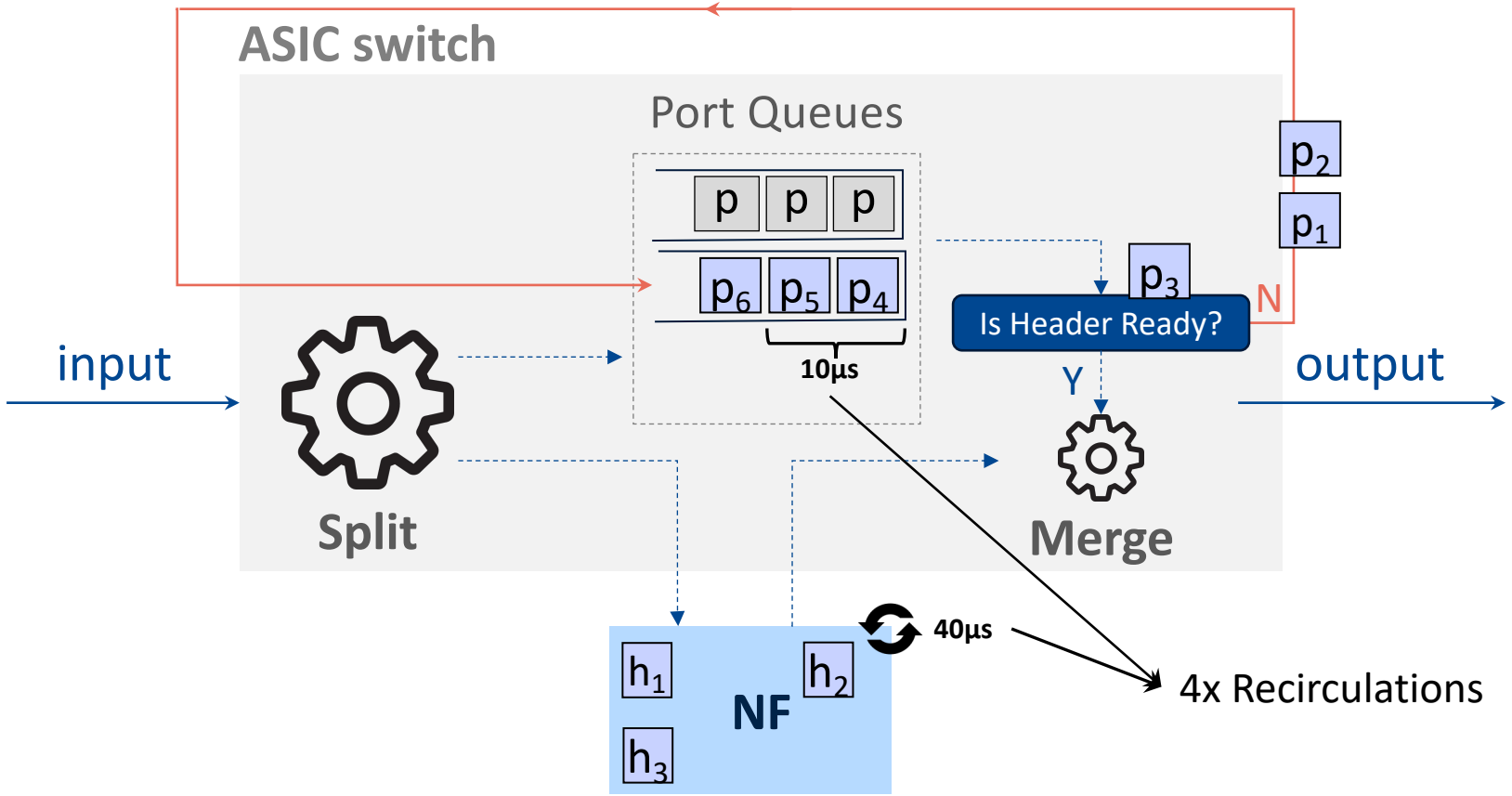
Recirculate payloads until headers are ready

Create copies of payloads to fill up the queues

Queue **self-clocking**

At steady state, # recirculations is predictable

Queue latency converges to the correct value w/o setting any parameter!



TurboSwitch

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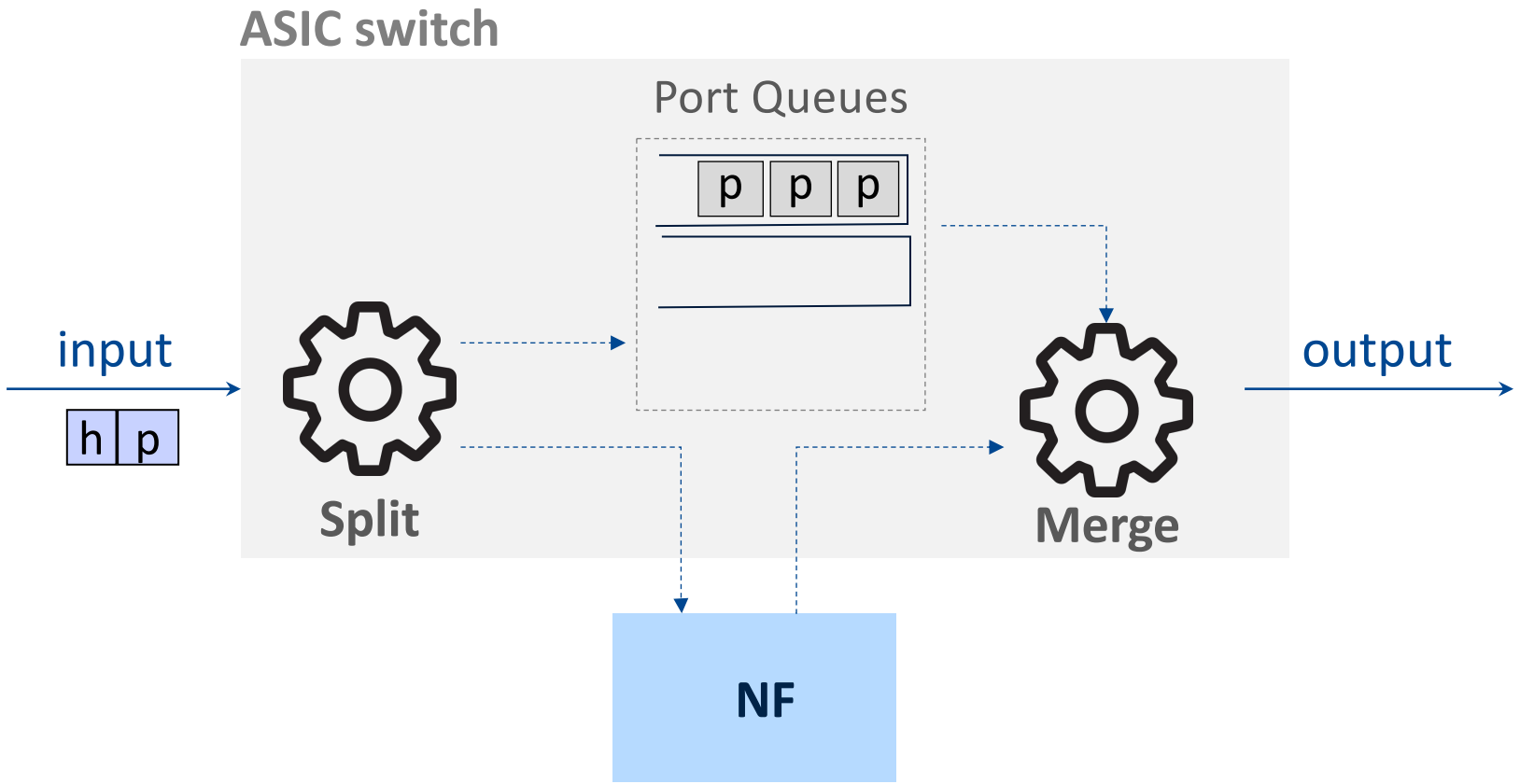
Recirculate payloads until headers are ready



TurboSwitch

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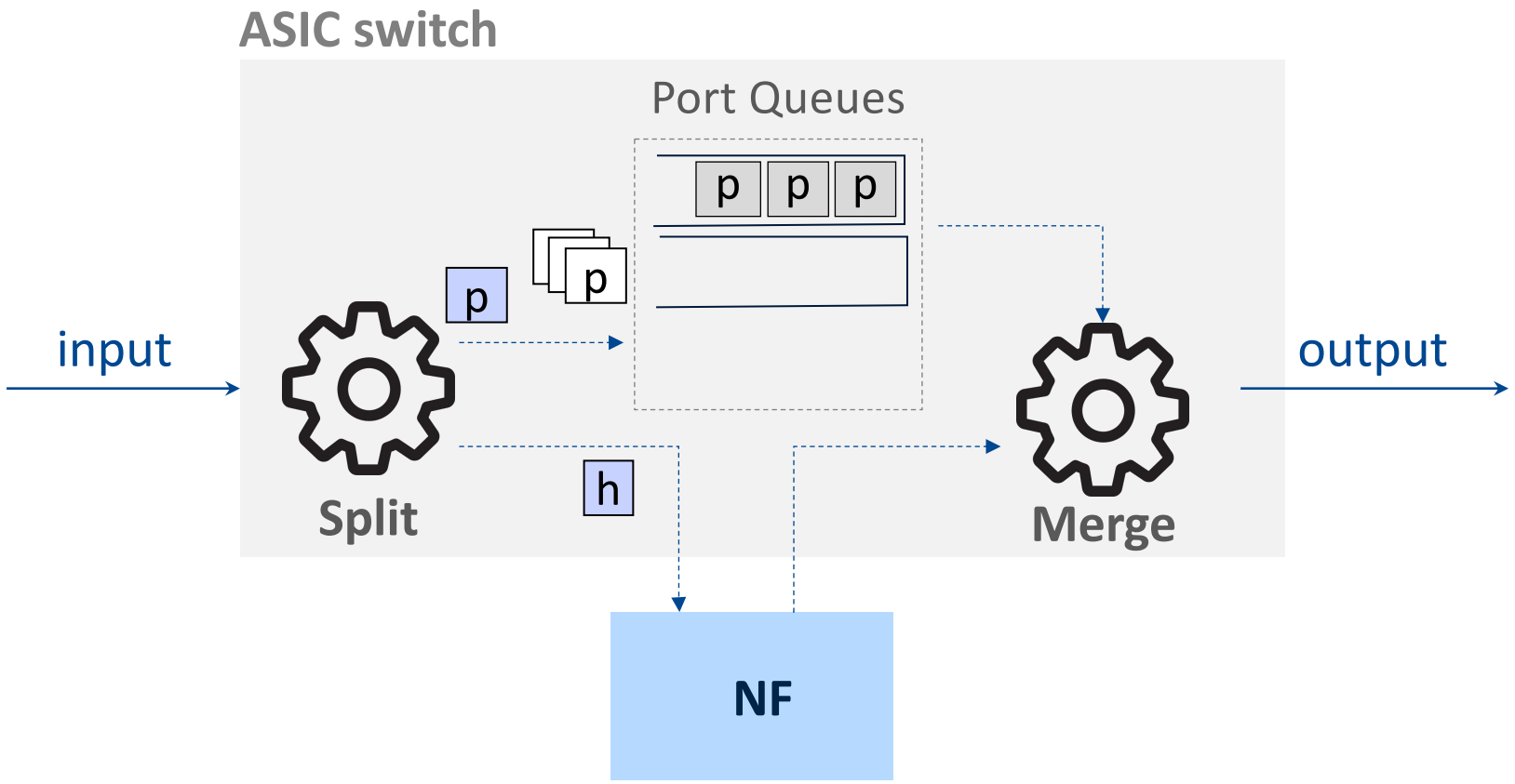
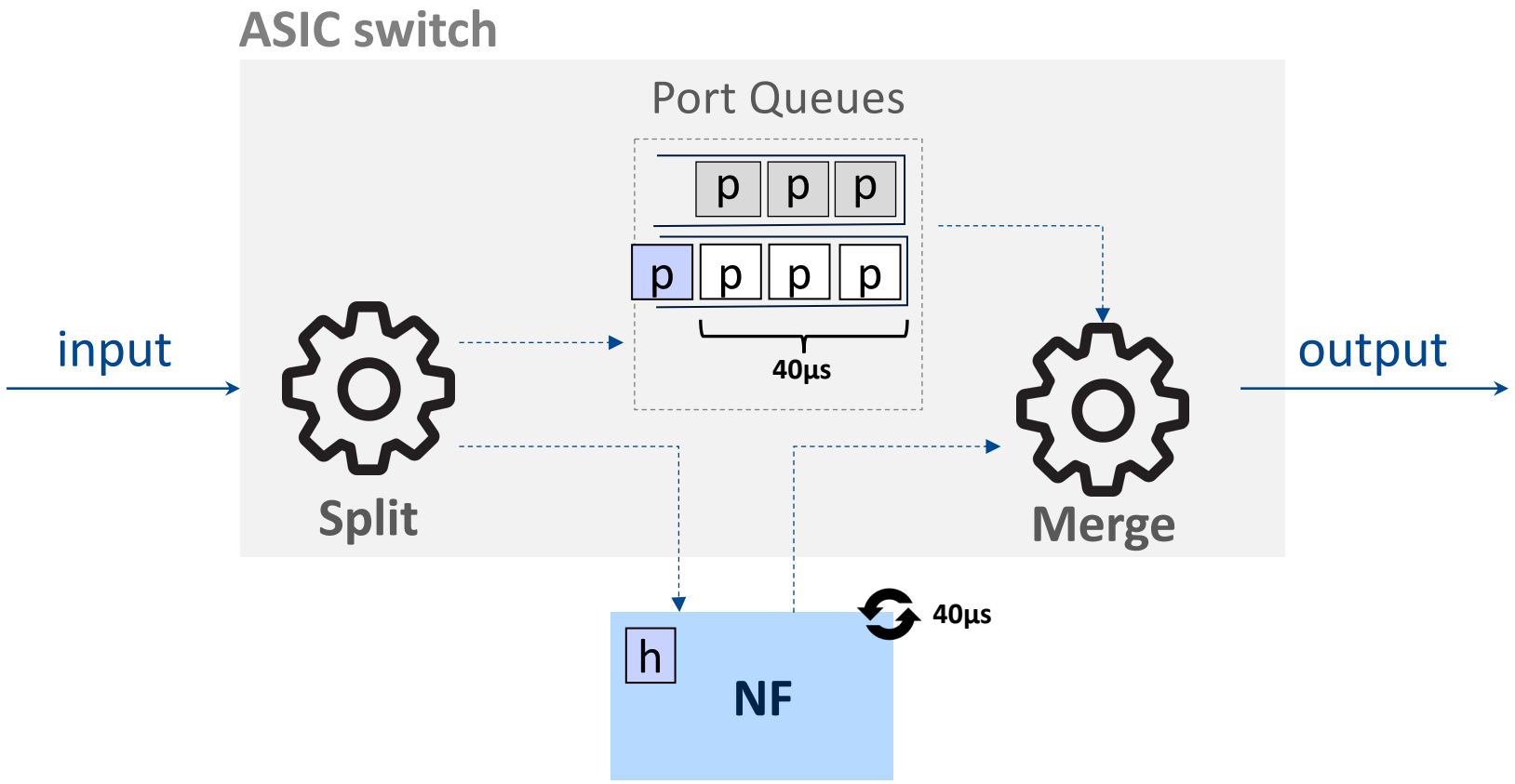
Recirculate payloads until headers are ready



TurboSwitch

Create copies of payloads to fill up the queues

Recirculate payloads until headers are ready



TurboSwitch

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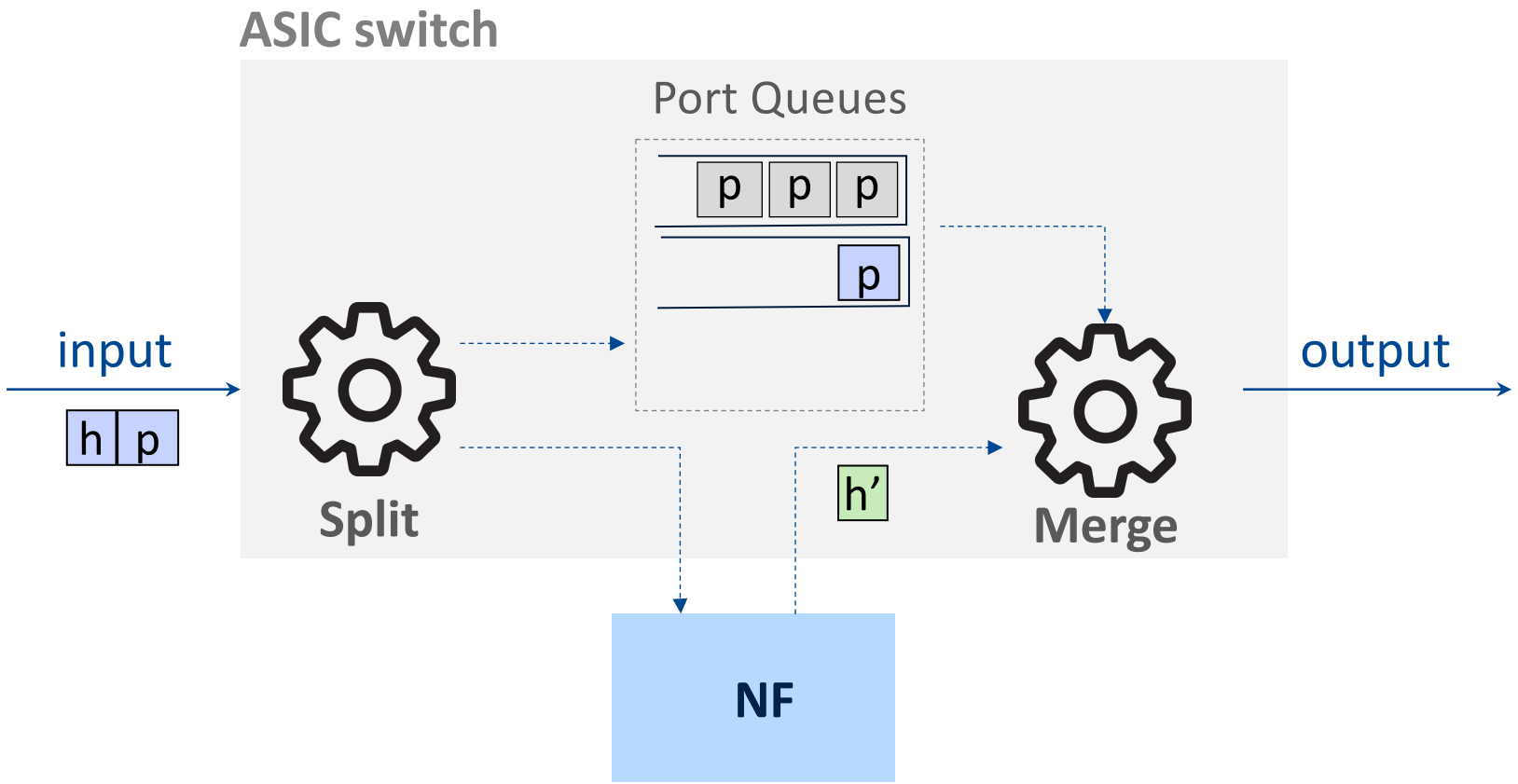
Recirculate payloads until headers are ready



TurboSwitch

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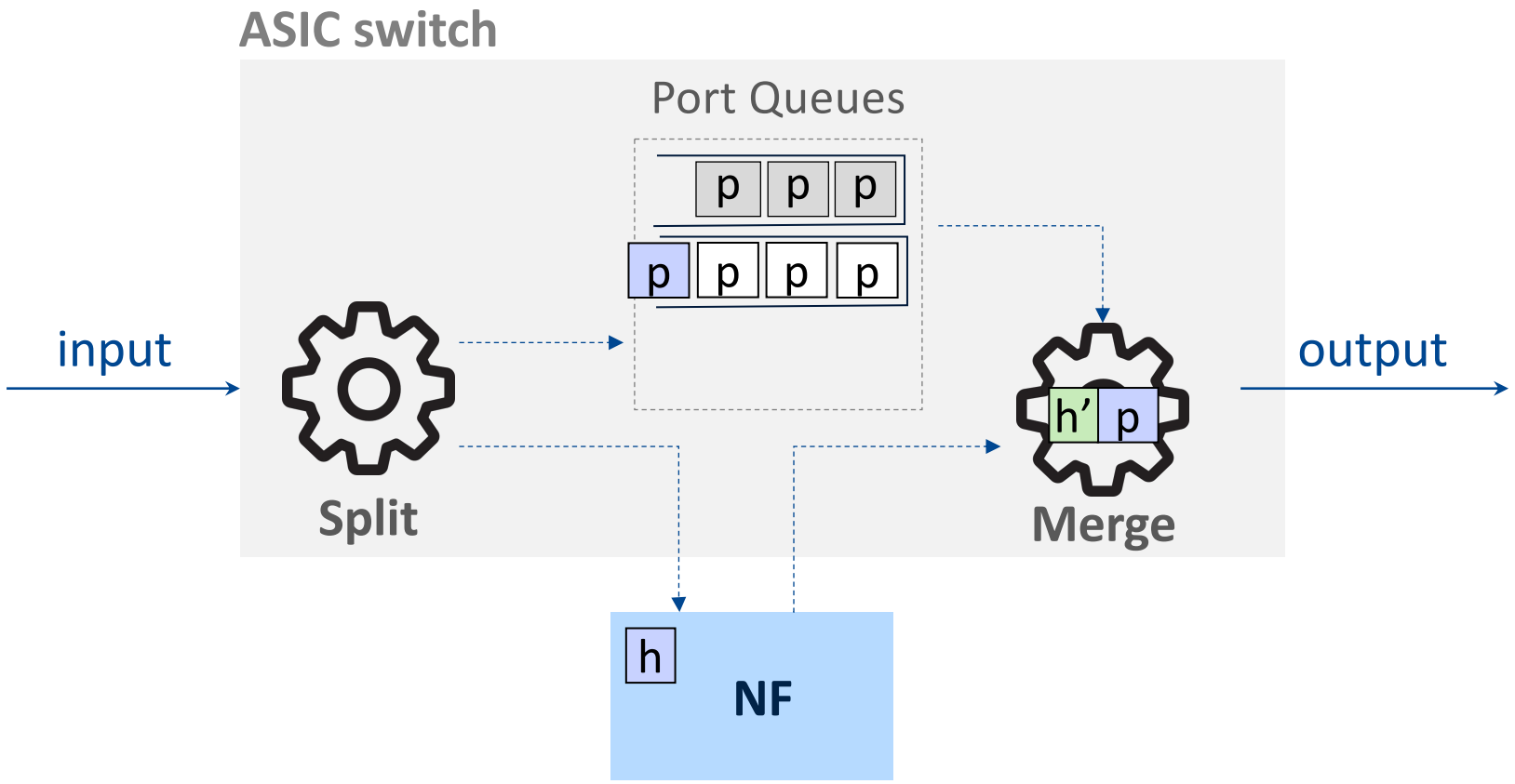
Recirculate payloads until headers are ready



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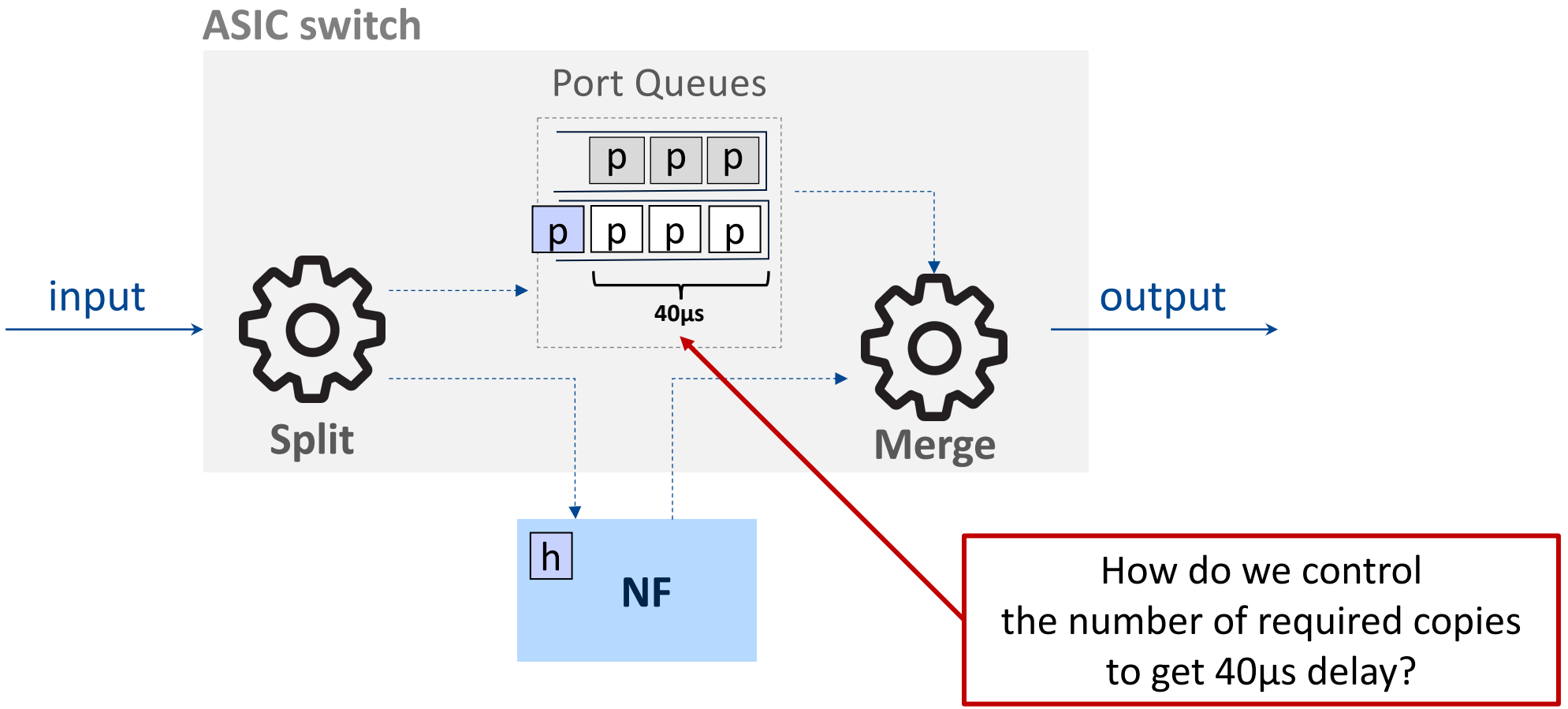
Recirculate payloads until headers are ready

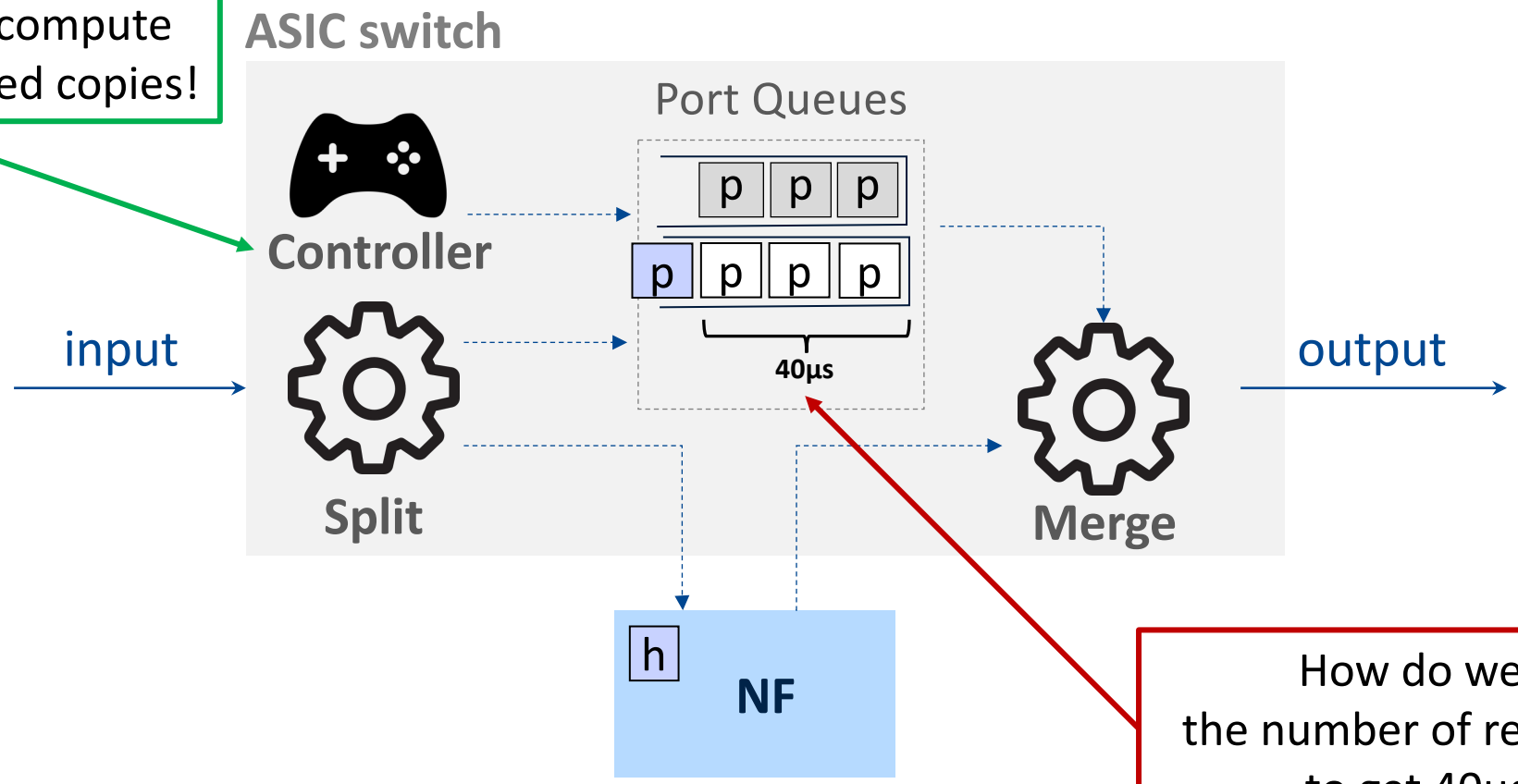


TurboSwitch

Create copies of payloads to fill up the queues

Recirculate payloads until headers are ready

Use Queue Stats to compute the number of required copies!



How do we control the number of required copies to get 40µs delay?

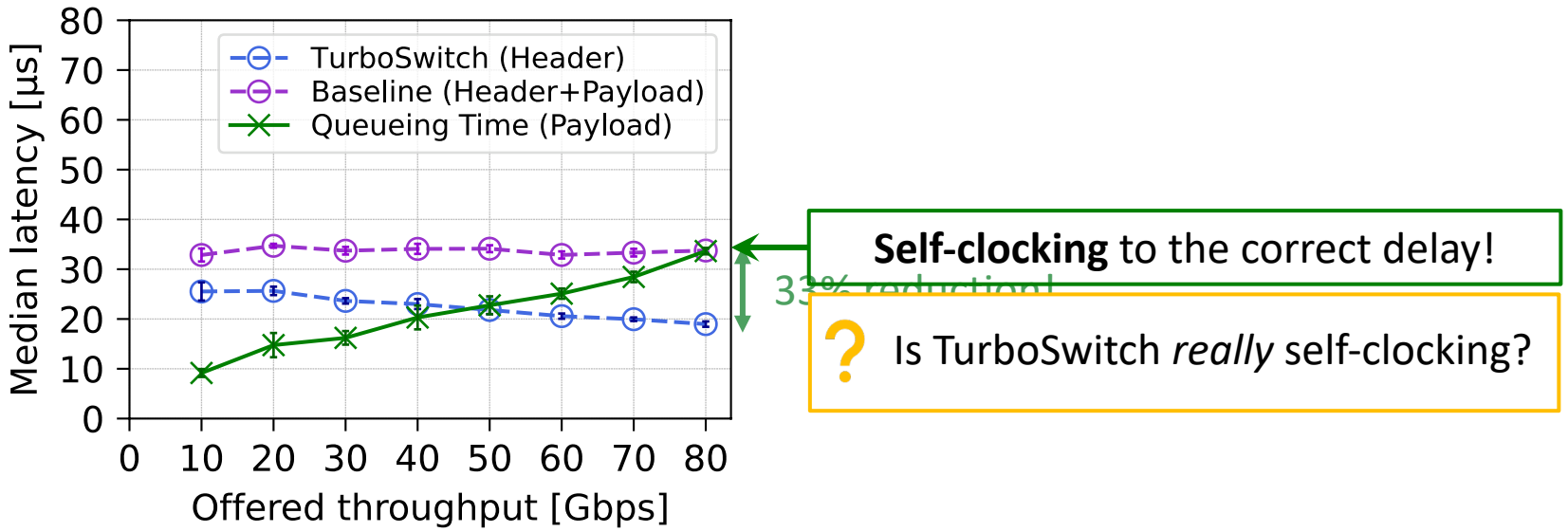
Evaluation

Evaluation

Recirculate payloads

- Intel Tofino ASIC
- FastClick Forwarder NF ⟹ 20µs Average Latency
- 100Gbps wiring

What are the NF latency gains of TurboSwitch?

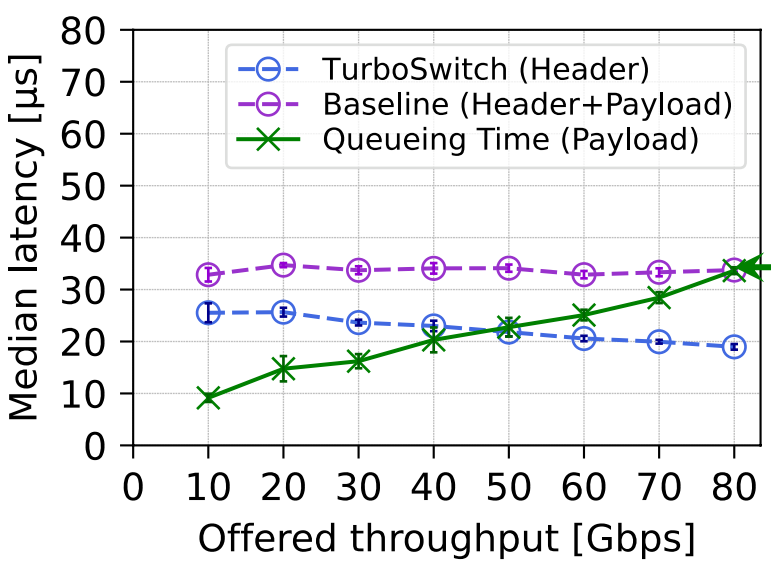


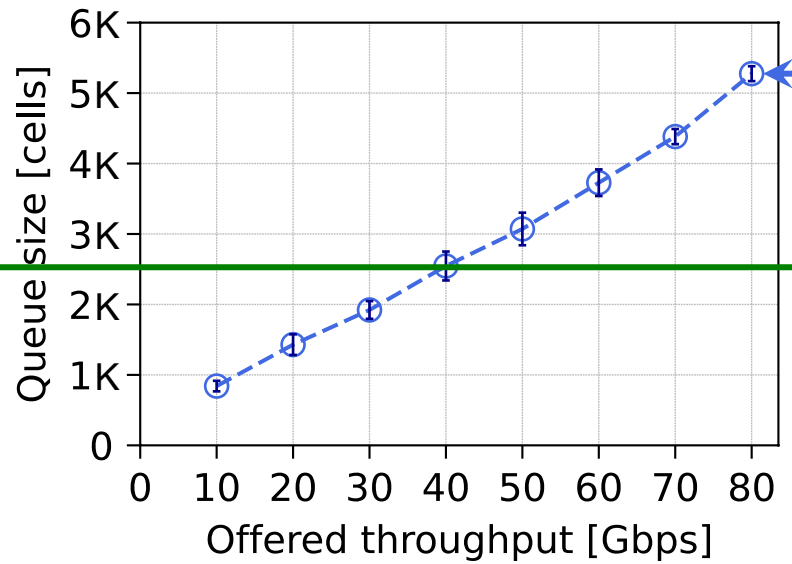
Evaluation

Recirculate payloads

- Intel Tofino ASIC
- FastClick Forwarder NF ⟹ 25µs Average Latency
- 100Gbps wiring

Is TurboSwitch *really* self-clocking?





Queue size grows linearly w.r.t. input throughput

Linear relationship between payload queueing time and queue size

Evaluation

Recirculate payloads

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- FastClick Forwarder NF ⟹ 25µs Average Latency
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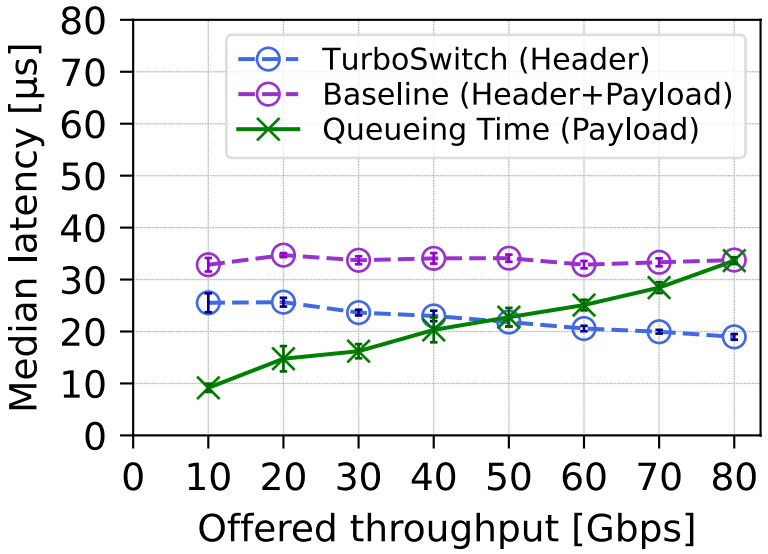

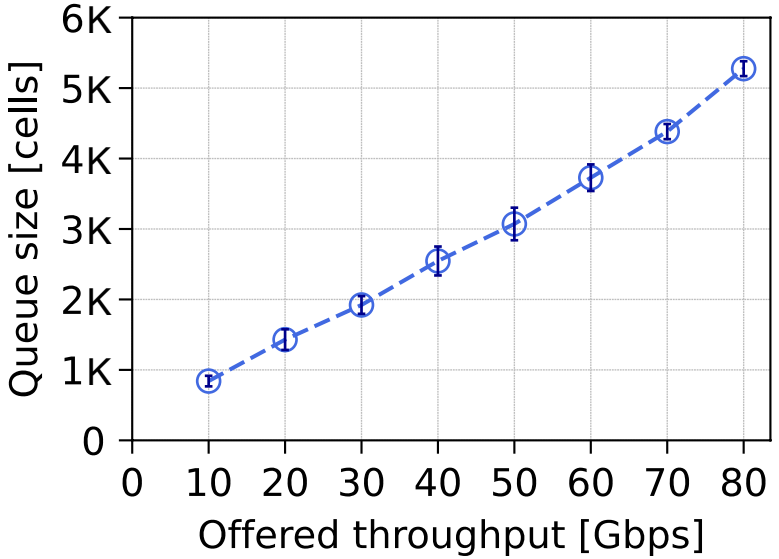

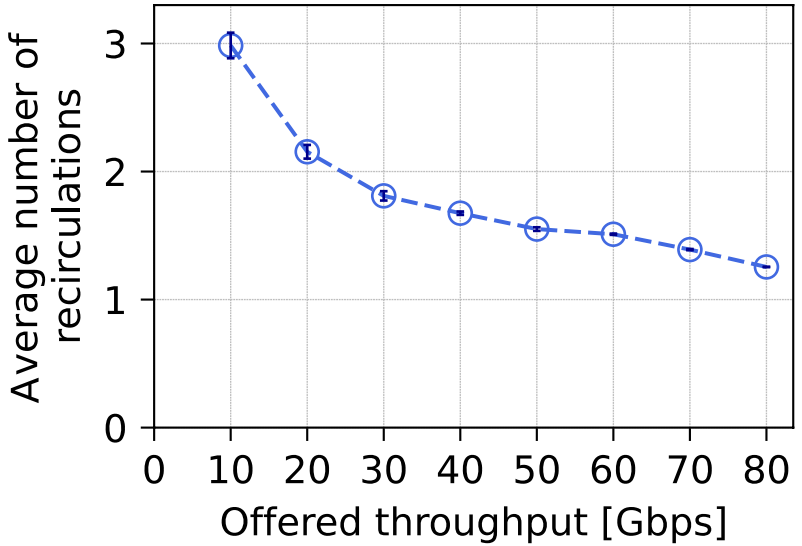

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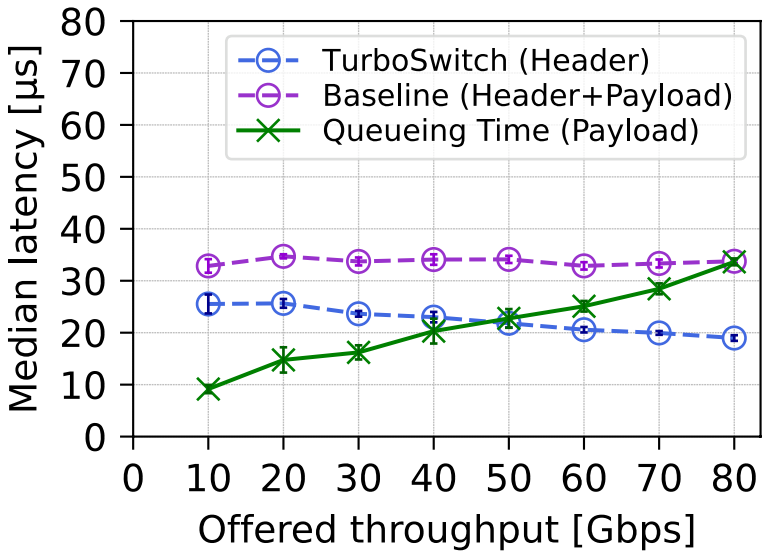
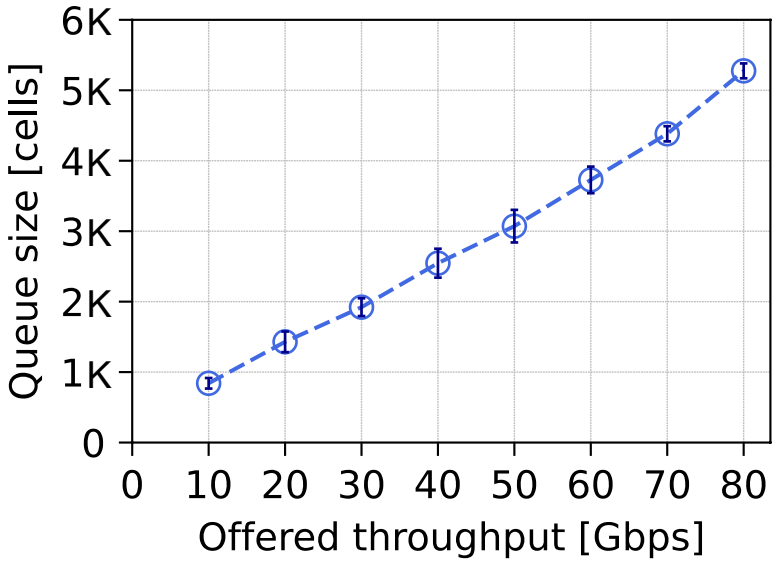
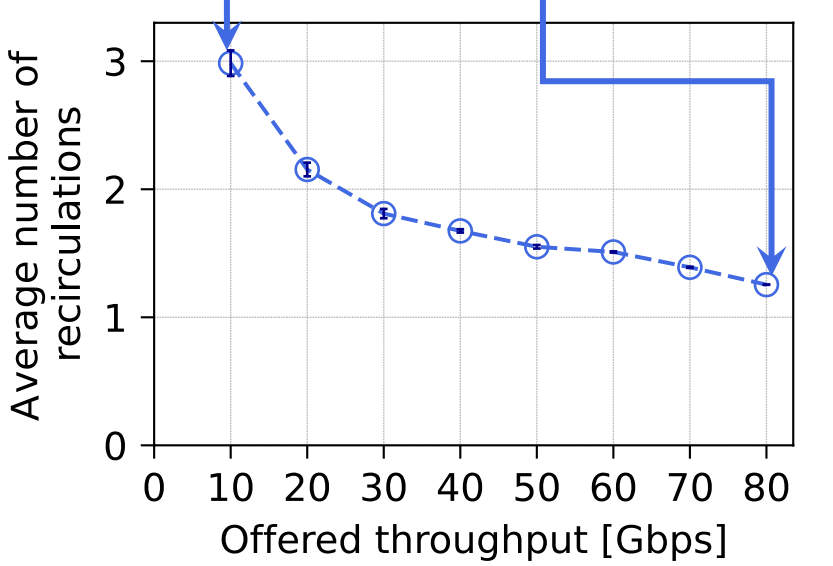


More recirculations
to keep a steady state



~1 recirculation per packet



Evaluation

Recirculate payloads

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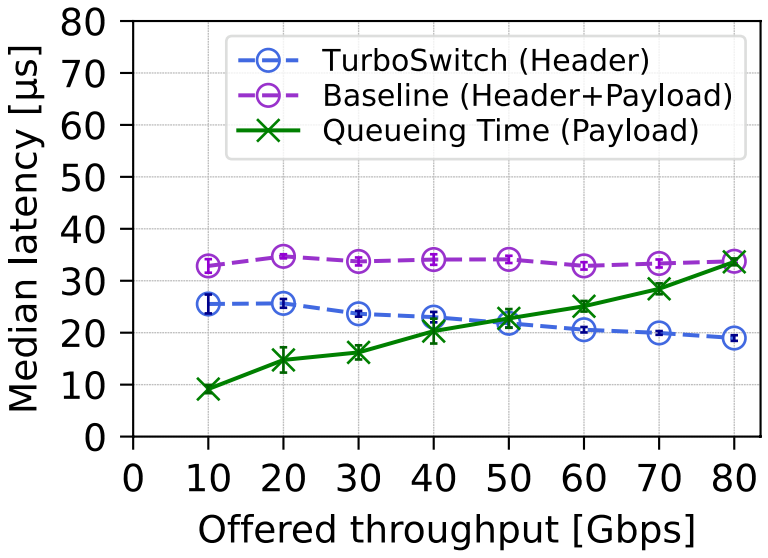
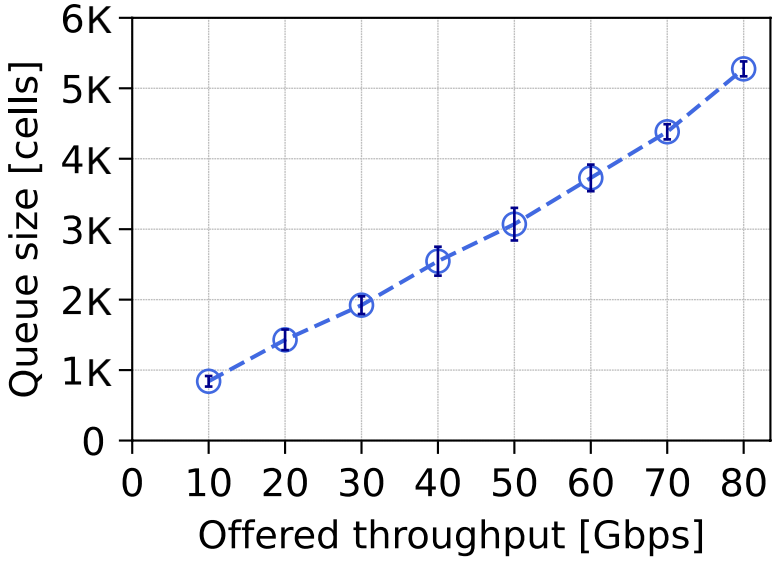
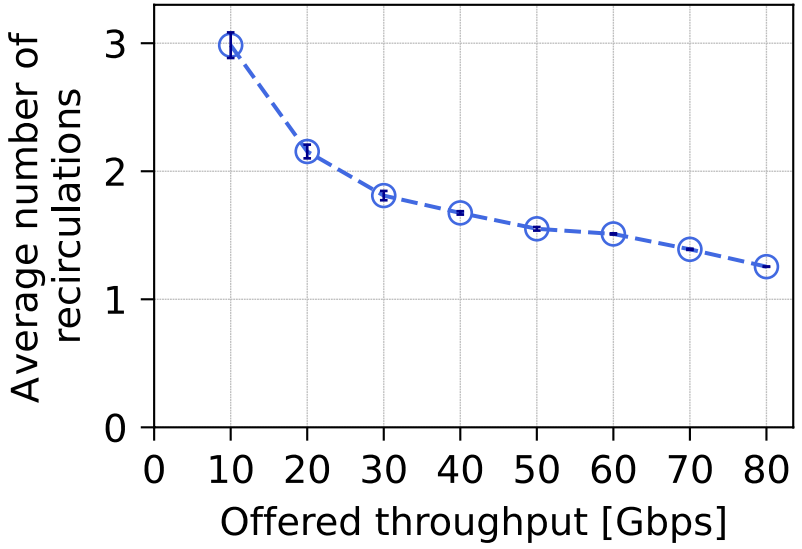
Is TurboSwitch *really* self-clocking?

Turboswitch **improves** NF performance by inducing **self-clocked congestion**!







Evaluation

Create copies of payloads

- Python Simulator – 20µs NF Processing Latency
- 100Gbps w/ Poisson arrival (64B-1.5KB pkt size)
- Controller ⟹ 1µs Queue Stats Update Delay

Can TurboSwitch's controller enforce the correct delay to payloads?

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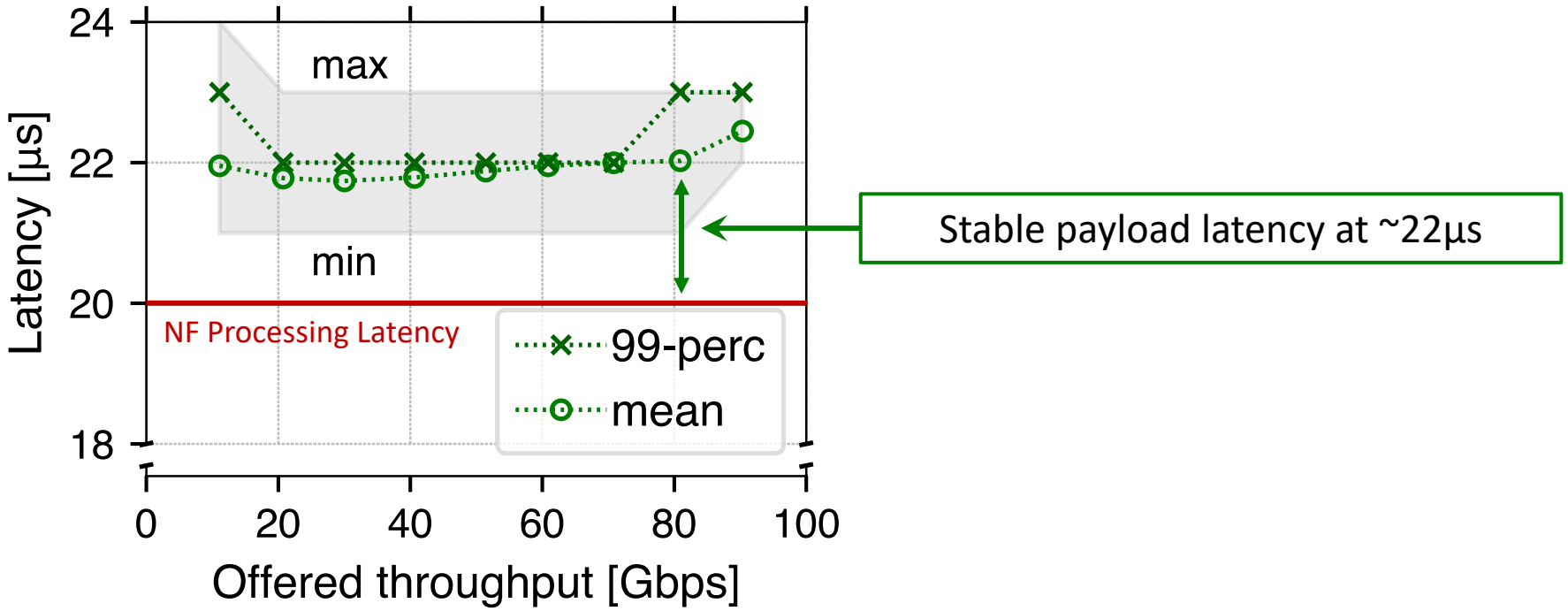

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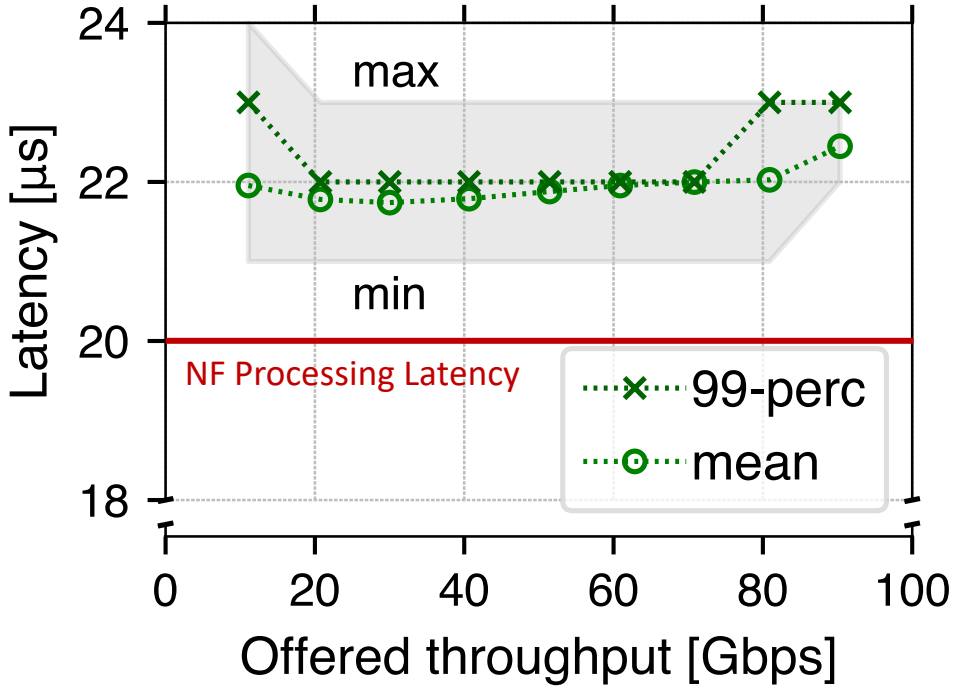

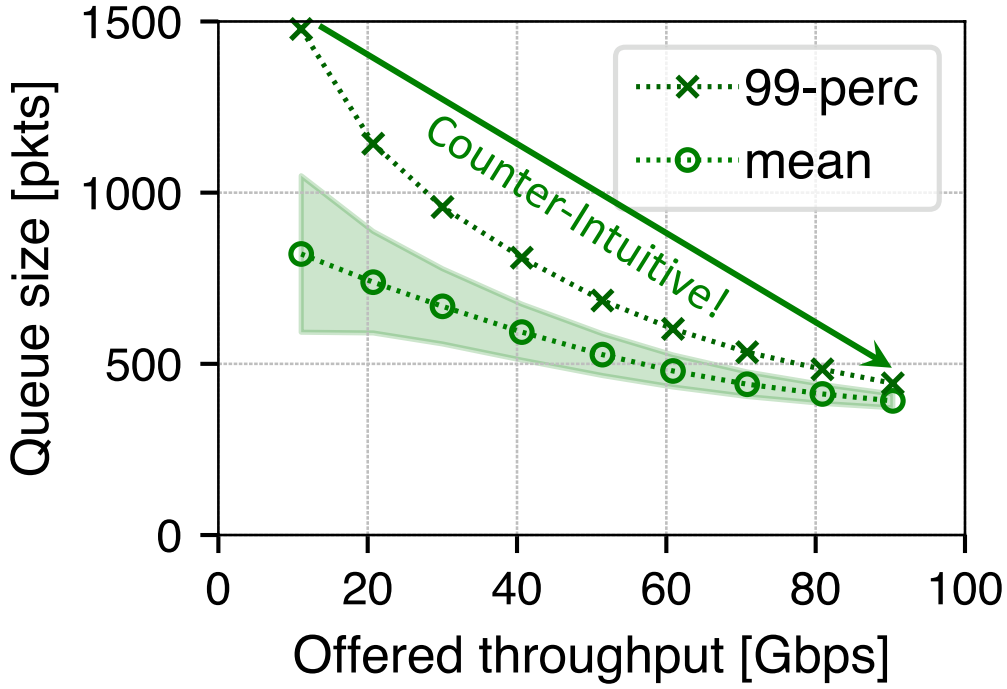

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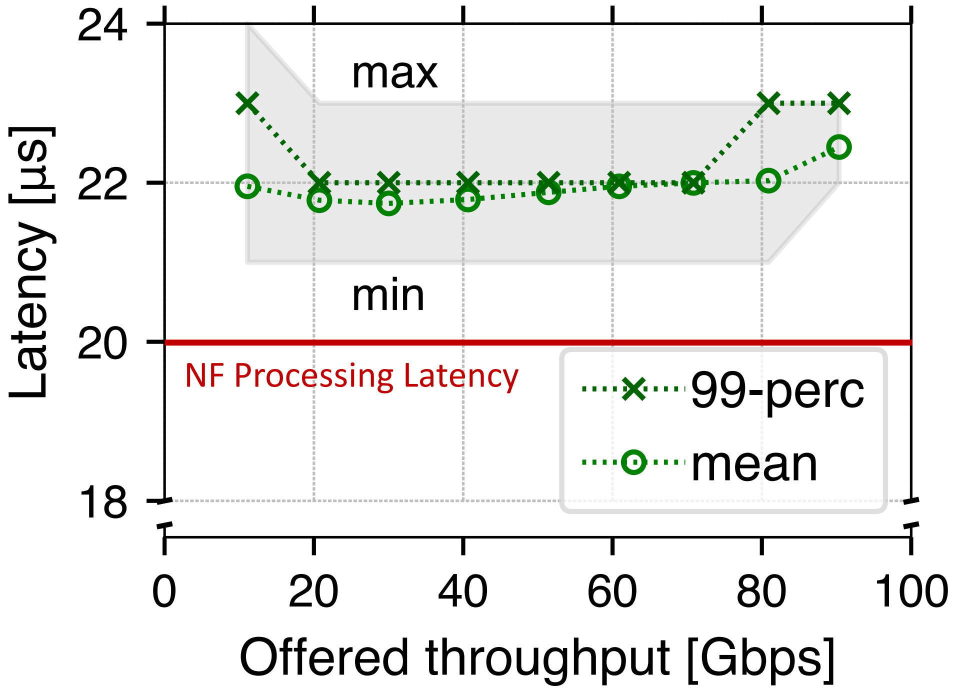
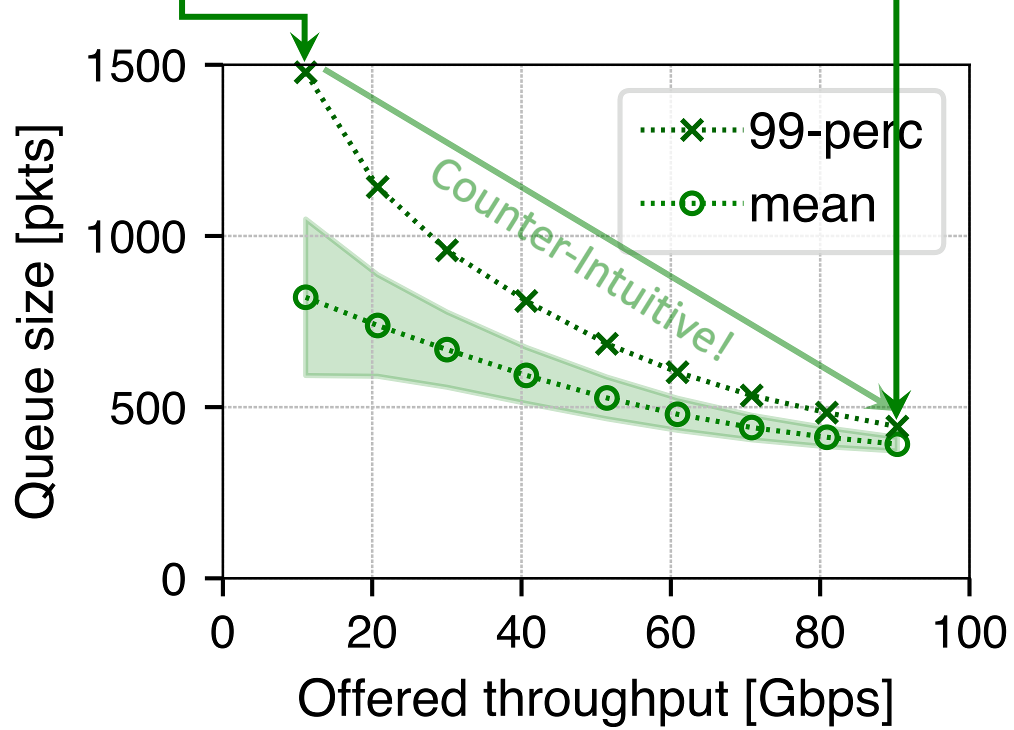


↑ **Less** incoming packets, controller creates **more copies**

↓ **More** incoming packets, controller creates **less copies**



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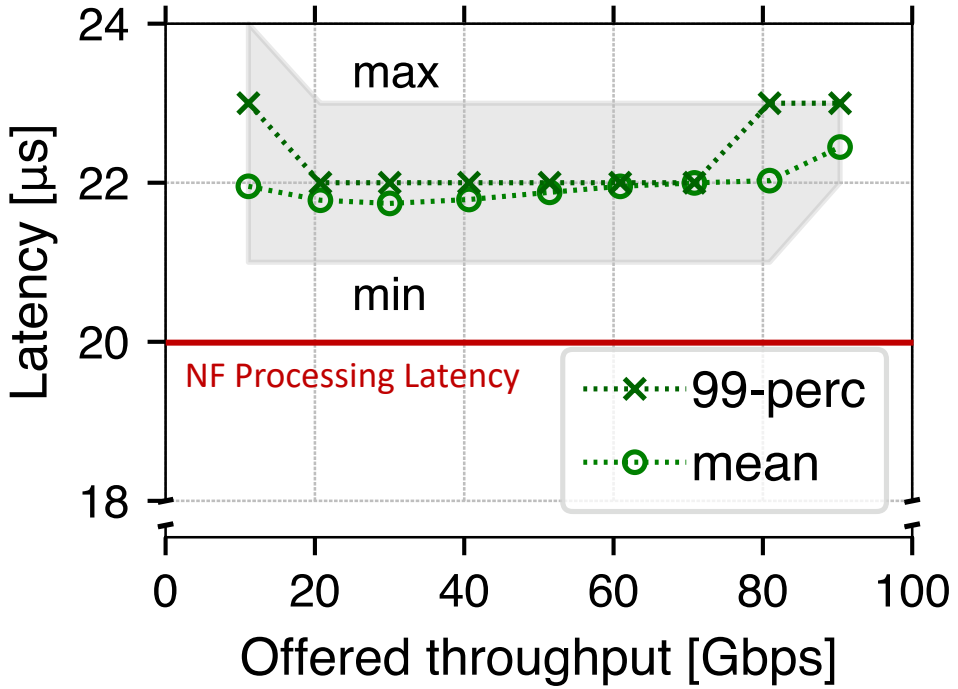
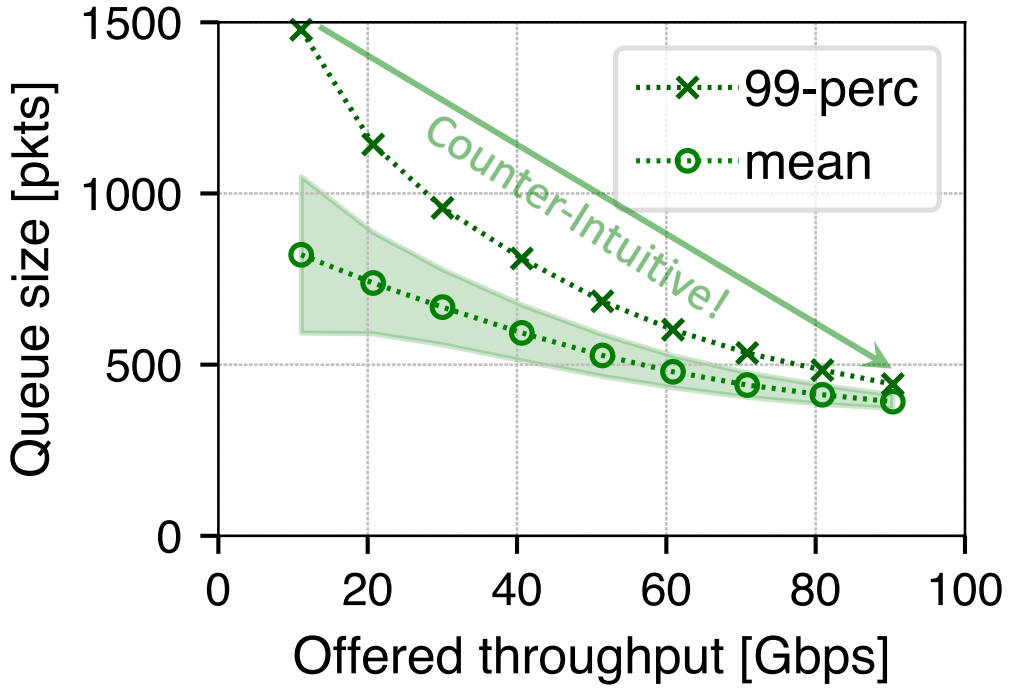
Can TurboSwitch's controller enforce the correct delay to payloads?

TurboSwitch **correctly sizes** queues to **enforce** the NF processing latency!





Conclusions

The **TurboSwitch** system:

- Presents a packet-splitting approach that **does not require external resources**
- Proposes a **queue-based buffer** to store payloads on existing ASIC switches
- **Reduces** NF processing time with **zero configuration**
- Spurs a question on whether **expose APIs** for controlling the forwarding buffer