

P4-NetFPGA

Stephen Ibanez, Gordon Brebner, Robert Halstead, Chris Neely, Nick McKeown

- Stateful P4 program support using externs inspired by Domino atoms
- P4₁₆ compiled to NetFPGA SUME platform using Xilinx P4-SDNet tool flow
- Demonstration: switch computes flow size distribution for TCP/IP flows
 - Fine grained analysis with per-flow counters
 - Inspired by FlowRadar

Atom	Description
R/W	Read or write state
RAW	Read, add to, or overwrite state
PRAW	Predicated version of RAW
IfElseRAW	2 RAWs, one each when a predicate is true or false
Sub	IfElseRAW with stateful subtraction capability
Nested	4-way predication (2 nested IfElseRAWs)
Pairs	Update a pair of state variables

Least Expressive



Most Expressive

DEMO:
Flow Size Distribution

